Analog Integrated Circuits
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Lecture - 36
Folded- Cascode OpAmp – 5

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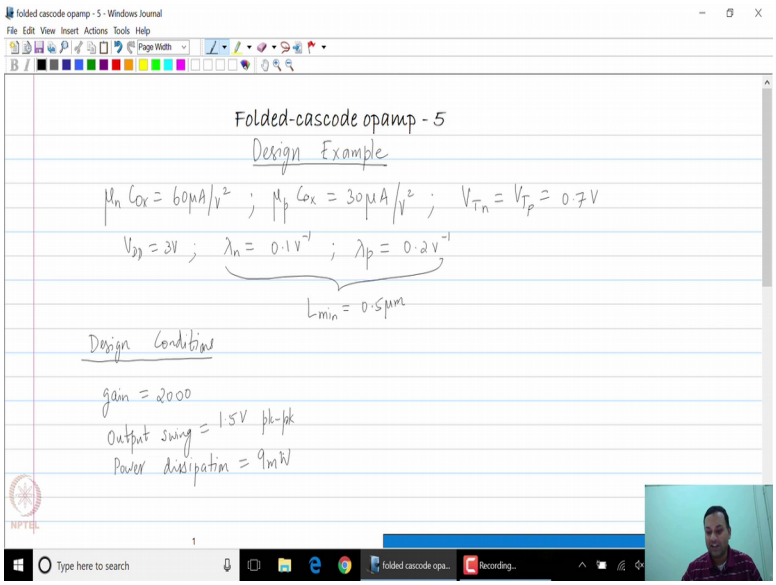

In this lecture we are going to do a small design example of the folded cascade opamp. So, let us say, let us take some sample parameters as well as design requirements.

So, let us start let us first start off with the transistor parameters. Let us say the you are given mu n Cox as some 60 micro amp per volt square mu p Cox it is approximately half that. So, 30 micro volt square and let us say the threshold voltages of the NMOS and PMOS are equal and 0.7 volts each. And let us say that V DD the supply voltage is 3 volts and we also need lambda. So, let us say lambda n is 0.1 volt inverse and lambda p is equal to 0.2 volt inverse and both of these are given for the minimum length of 0.5 microns. So, clearly lambda s has to be specified for a value particular value of length of the transistor.

And the requirements, so design conditions, so to make our design look more like real world design we are not going to over design you know over constrain because we do not we want to come up with an initial design based on some smaller subset of the real world conditions. So, let us say that we need an overall gain of 2000 and the swing limit.

So, let us say I need an output swing of 1.5 volts peak to peak and I am going to give one more condition which is the power dissipated the power dissipation in the circuit, let us say has to be in the core circuit has to be 9 megawatts.

Now, we want to see how to start off with these and come up with a design sample with a particular design and as you might imagine you have done earlier we are not going to set up some you know a certain set of equations and try to solve variables because it is much easier to iterate than to you know set up the design conditions. So, that is kind of the system that we are going to follow.

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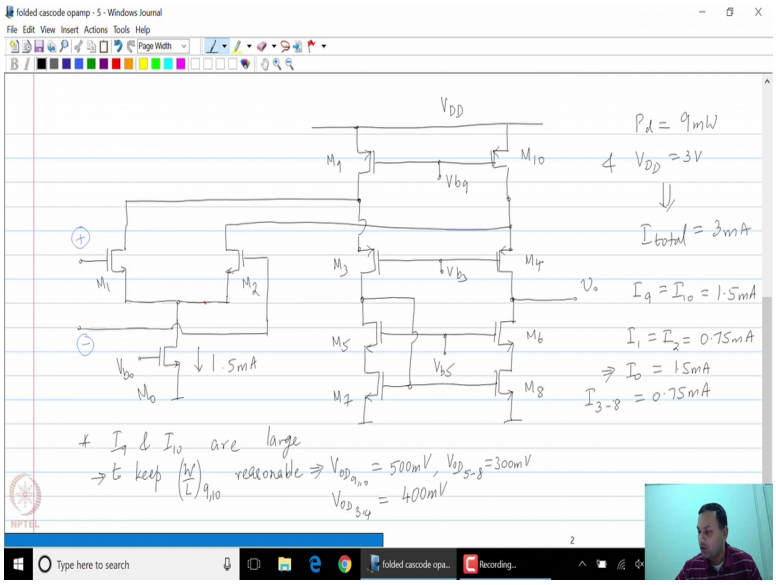

So, let us look at the circuit that we have been looking at we will assume that you are going to use folded-cascode opamp with an NMOS n input pair. That will clearly be decided by the input common mode requirements the NMOS and the PMOS input packs will have different input common more levels.

Now, let us say that we start off by taking the power condition. So, the power condition says that this power dissipated is 9 milliwatts and V DD is 3 volts. So, both of these together tell us that the total current that can be drawn from the supply is 3 milliamps and where does this current come from clearly this correct comes from supply and flows through M 9 and M 10.

So, therefore, we are going to say I 9 is equal to I 10 is equal to 1.5 milliamps. So, we are going to give 1.5 milliamps to I 9 and I 10 the total current drawn from supply will then be 3 milliamps we will be within the power budget. So, once we have decided this we now need to decide how much of this is going to go into the different paths. So, let us say that we are going to divide the current equally between the 2 paths. So, let us say this path is going to have 1.5 milliamps of current in other words these two I 1 and I 2 are going to be 0.75 milli amps each. So, and I 0 is clearly 1.5 milliamps and of course, then I 3 to I 8 are all going to have 0.75 milliamps each.

So, now we have set the bias conditions perfectly well we have decided that M 1 to M 8 all these transistors are going to have 0.75 milliamp each, M 0 is going to have 1.5 milliamps, M 9 and M 10 are going to have 1.5 milliamps. So, we have now decided the bias currents.

So, the next step we have used one condition which is the power which is the power dissipation constraint. The next step now is to come up with an optimum with a width and length of the device we are going to arrive at this from the condition for output swing. So, now let us take the output voltage. Now, as you can see we need to give a certain amount of swing for the upper transistors and the lower transistors we are going to apply the swing condition to come up with the devices.

So, the first thing we will note is that I 9 and I 10 are the largest currents in the circuit. So, we are going to say that because we do not want M 9 and M 10 to become too large we are going to say that we are going to give them a large V S D sat and large over drive to work with. So, to keep the size as reasonable right we are going to say V S D sat or I will just call it V overdrive which is exactly the same thing. So, V overdrive of we are going to say we will give it 500 millivolts and remember that the output common mode is very often under our control. So, we are going to say that we can with the output common mode does not have to be at V DD by 2 we are now going to say that V OD 9 and I am sorry V OD 3 and 4 is 400 millivolts because these are part of the cascode path common gate path we are going to give it slightly higher overdrive. M 5 to M 8 are purely having a current mirror action. So, we are going to give them 300 millivolts each. So, we are going to give up 300 millivolts each.

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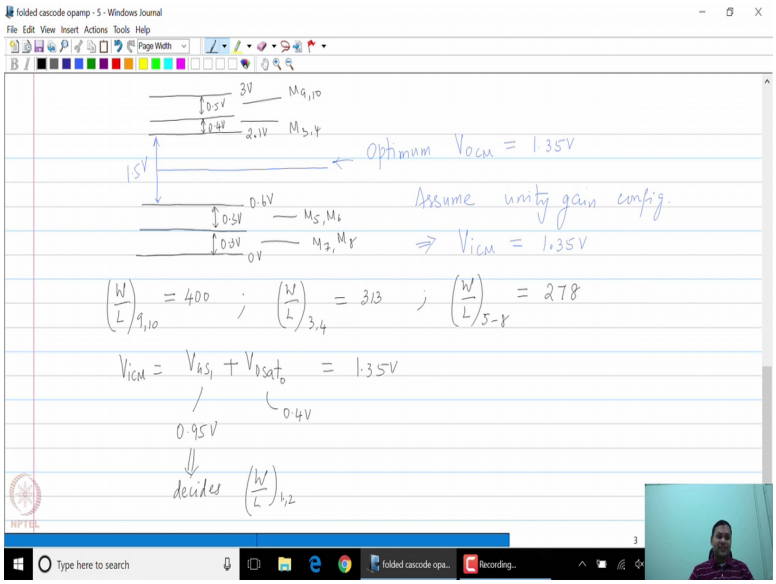

So, if you actually look at the output levels the swing, the output is going to swing between 2 levels you have V DD minus V overdrive of 9 and 10. So, this is V DD which has 3 volts and you are giving slightly more than half of that to M 9 and 10. So, you are going to give them 0.5 volts for M 9 and 10. So, and we have now given 0.4 volts for M 3 and 4 so; that means, your maximum voltage at the output can be 2.1 volts.

Now, what about the bottom side? On the bottom side we have now split the overdrives. So, this is ground we have now said you are going to give 300 millivolts. So, 0.3 volts to M 5 M 6 and M 7 M 8.Now, therefore, the input common mode is sorry not input common mode the lowest level is at 0.6 volts. Now, that gives us 1.5 volts of allowable swing which is exactly what we wanted, we have 1.5 volts peak to peak allowable speed.

Now, the other thing we can derive from this now that we have apportioned the overdrive voltages we can also see that the ideal common mode voltage at the output should be somewhere exactly in between. So, the optimum output common mode voltage should be exactly in between these two which happens to be at 1.35 volts. So, the output should be biased at 1.35 volts. Now, to work backwards we are now going to assume that the opamp needs to operate at unity gain, which means the input common mode would be at around 1.35 volts.

Now, this helps us set values for the input also. So, before we go there let us fix now that we have fixed the overdrives of all M 3 to M 10. Let us now derive the W over L we are

going to derive the values of W over L. So, W over L of 9 and 10 because we have fixed the currents and overdrive voltages you can calculate this it turns out that W over L of 9 and 10 would be 400, W over L of 3 and 4 would be approximately 313 and W over L of 5 to 8 would be 278 approximately.

So, the once you have fixed this we can now come up with the input levels also now since we have said unity gain we will now say that V icm has 2 portions, one is the V G S of the input device and the V D sat of M 0 and this have to be 1.35 volts. And now we are going to do somewhat arbitrarily say this is going to be 0.4 volts and this is going to be 0.95 volts

If we fix it this way this will decide the V G S 1 and the W over L of M 1 and M 2 also. So, this will give you M 1 and M 2. Now, you have all the sizes width to length ratios of all transistors in the circuit because you have now used the power dissipation condition and the over drive swing limit conditions to arrive like this with some certain logical reasonable assumptions.

So, now the next step is to calculate the gain of this particular opamp.

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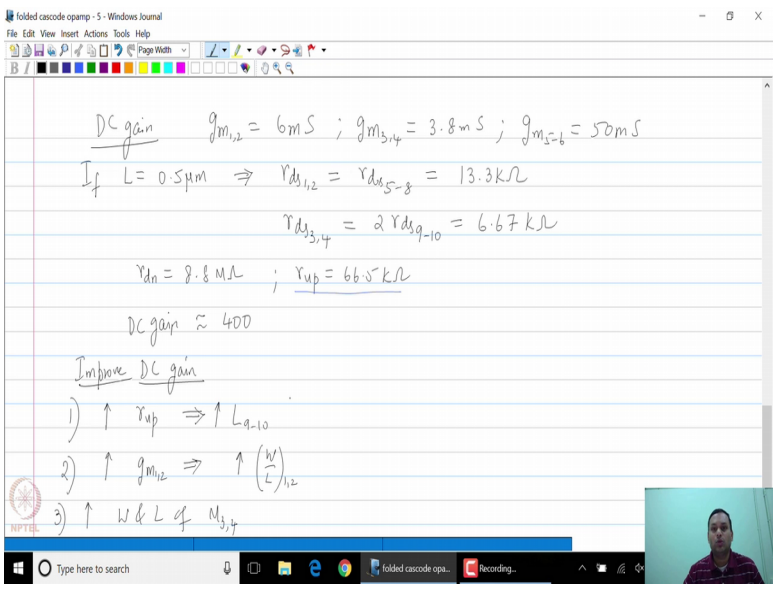

Let us calculate the dc gain to calculate the dc gain we are now going to decide the g ms of the devices and as you can see W over L 1 and 2 we will get a number of approximately 400 for this and that will help us decide the g ms of the devices. So, g m

of 1 and 2 would be approximately 6 millisiemens gm of 3 and 4 would be approximately 3.8 millisiemens and gm of 5 and 6 would be approximately 50 millisiemens.

And let us assume that, let us start off assuming here trying to use minimum length which is what you would do because you want to keep the parasitic capacitances as small as possible. So, we are trying to find out if that would work for us. So, if L is equal to 0.5 microns this tells us that r ds of 1 and 2 would be the same as r ds of transistors 5 to 8 these would be approximately 13.3 kilo ohms, r ds of 3 and 4 would be twice r ds of 9 and 10 would be equal to 6.67 kilo ohms.

Now, note that first of all the lambda of the PMOS transistor was already larger. So, you expect the output resistance to be worse you have designed them to have the same currents and therefore, the intrinsic gain of 3 and 4 of devices 3 and 4 are actually quite small. So, please note that if you actually find out gm 3 times r ds 3 that ends up being quite small. So, this is you will soon find that this is going to affect us.

So, let us calculate the impedances looking up and down. So, the impedance looking up is r up and the impedance looking down is r down. The overall output resistance is r up parallel r down. So, it turns out that for this particular circuit r down is 8.8 mega ohms r up is 66.5 kilo ohms.

As you can see because of the limited intrinsic gains of you know the PMOS transistors your upwards impedance is much much smaller than the downward looking impedance and as you might expect since this is skewed in one direction the gain DC gain of the opamp ends up being only about 400 which is very far away from 2000. So, you will now have to iterate for the gain.

Now, the iteration needs to go in a reasonable direction. So, now, we need to figure out what is causing this lower gain. As you can clearly see the first thing that you need to do is fix this right. If you increase r up you will be able to get better DC gain because that is limiting the value of DC gain. So, the first thing that you would do is. So, we now want to improve this DC gain. So, the things we will have to do. The first thing we want to do is increase the upwards looking impedance so that the overall output also increase. And this can be done in several ways you want to consider first because r ds 9 and 10 is 3.33

kilo ohms which is extremely small you first want to increase r up. So, increase L 9 and L 10 to increase the impedance looking upwards. That is the first thing you would do.

Note that; that would increase parasitic capacitances at various modes in the circuit. So, the bandwidth of the opamp needs to be kept in mind while doing this. So, the second thing you can do is increase g m 1 and g m 2 because as you can see for a gain of 2 thousands g m 1 2 of 6 millisiemens is actually quite low. So, you want to increase g m 1 and 2 which means increase W over L of 1 2 because you do not want to increase the power dissipation.

Note that again this would increase the parasitic capacitance at various nodes in the circuit. And number 3 you want to increase W and L of M 3 and M 4 because the intrinsic gain is very small. So, this of course, again would increase to, would increase the various parasitic capacitances in the circuit. So, now, you can use a combination of these 3 you know procedures to increase the gain, to increase the gain to the required value of 2000.