Analog Integrated Circuits
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Lecture – 35
Folded- Cascode OpAmp – 4

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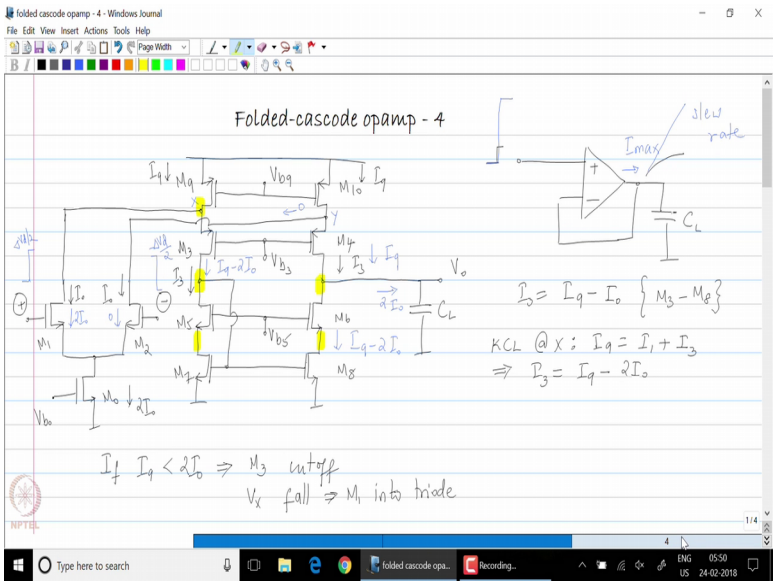

In this lecture we are going to study the folded-cascode opamp a little bit further because there are a few more things to understand about the folded-cascode opamp. The 3 major quantities that we still have to look at are the slew date of the opamp, the noise input referred noise and the input refer offset and finally, we need to build the datasheet of the opamp in an organized manner as a table. So, let us first start off with each one of these one by one.

So, the folded-cascode opamp that we will draw is an NMOS input path, folded-cascode opamp. We will assume this has the high swing cascode on the NMOS side. So, let us number the transistors M 1 and M 2 are the input path M 0 is the current source, M 3 and M 4 or the common gate transistors. So, they have a gate bias voltage of V b 3. M 5 to 8 found the NMOS current better at the bottom and there is a bias voltage V b 5 at that k and finally, M 9 and M 10 are the current sources and they have a bias voltage V b 9 let us assume that the output has some load capacitance C L and the output is taken at the

common drain node between M 4 and M 6. We have seen the structure before. So, let us now look at the slew rate of this opamp.

To do to look at the slew rate let us quickly review what slew rate is. So, when you are looking at the slew rate of the opamp you for example, you might be in unity gain feedback and you are driving a capacitive load let us say and you apply smaller and smaller larger and larger input steps and it turns out at some point of time the output will not be able to follow. And eventually the output will not be able to follow in the small signal fashion and because there is a certain limitation on the rate at which the capacitance C L can be charged that is given by the maximum. So, when the input step gets really large the output current of the opamp cannot support such a large rise time and there is some maximum output current that the opamp can deliver and at this stage the output rises linearly. So, the output rises linearly and more importantly any large any larger input step will not allow the output to rise faster than this ramp. Now, this is called the slew rate of the opamp.

Now, let us we have seen the slow rate of the regular 5 transistor one stage opamp as well as the telescopic opamp. So, let us quickly look at the case for the folded-cascode because there is one small difference between the folded-cascode and the other opamps. So, let us assume that the total current through M 0 is sum 2 I naught. So, therefore, the in the regular bias conditions the 2 currents are I naught each let us assume that the current through I 9 and I 10 are I 9. So, I have a current I 9 through I 9 and I 10. So, based on the value of V b 9 that I choose and of course, the bias current through M 3 M 5 M 7 and M 4 M 6 M 8 are each going to be. So, let me call that I 3. So, I 3 is simply going to be I 9 minus I naught.

So, this is going to be the design condition the bias point for each of these transistors. So, I 3 flows through M 3 to M 8, these 6 transistors. So, clearly I 9 has to be larger than I naught that is we have seen. So, now, let us assume that for this particular opamp we apply a very large input step. So, in other words the input differential voltage has a very large step, so delta V d at the input. When this happens let us assumed this is a positive step. So, that the gate of M 1 goes very high gate of M 2 is cool very low when this happens. So, let me show that in blue color. So, delta V d by 2 I (Refer Time: 07:21) and minus data V d by 2. So, that there is a large delta V d are the input.

When this happens the current through M 1 will become 2 I naught the current through M 2 will become 0. So, if delta V d was large enough all of the current would flow through an M 1 and then we know current through M 2. So, now, what happens at let me call these 2 nodes node x and node y. If you look at node x there is a current entering which is I 9 and there is a current which is leaving which is equal to I 3 plus I 1. So, KCL at x tells you that I 9 is equal to I 1 plus I 3 when these subscripts denote the drain current of transistors corresponding to those numbers. So, in other words I d 9 is equal to I d one plus I d 3.

Now, I 9 of course, is fixed and now the current entering M 3. So, I d 3 now is equal to I 9 minus 2 I naught because I naught happens to be the original bias current through M 1 and M 2. Now, all of this total bias current 2 I naught goes through M 1. So, the important condition to note is that if I 9 was less than 2 I naught M 3 for example, would get cut off because it cannot support reverse currents I am naturally what this means is that V x and V y would fall to push M 1 into triode region. So, that would be the progression this is not something which is desirable. So, you need to ensure that I 9 minus 2 I naught is greater than 0.

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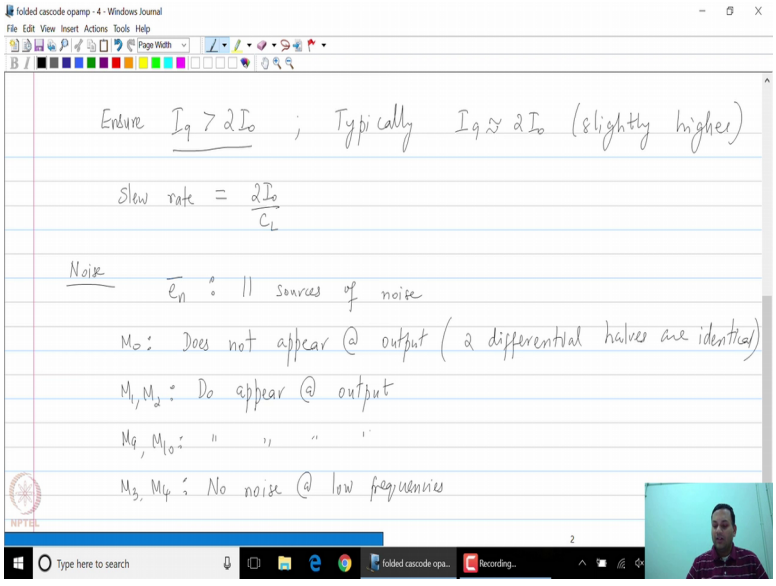

But of course, we do not want to burn 2 too much current. So, therefore, typically I 9 would be of this may be approximately 2 I naught and slightly greater. So, you have to ensure I 9 greater than 2 I naught, but you can just make it slightly higher than 2 I naught

so that no transistor he leaves the triode leaves the saturation region. So, this is something to be ensured if this happens.

Then you will have to find out what the total current through the output node is. So, let us assume that I 9 is greater than 2 I naught in which case the current through M 3 M 5 M 7 is equal to I 9 minus 2 I naught. And what happens to this current? This current of course, gets mirrored through M 8 and M 6. So, this current is clearly I 9 minus 2 I naught flowing downwards.

Now, what happens to the other path? M 2 is clearly cut off therefore, the current I 9 now completely flows through M 4 and M 10. There is no current I naught that is being pulled out of y into the input stage. So, this current is 0. Now, this means that a current 2 I naught flows through the load capacitance and therefore, the slew rate is equal to 2 I naught over C L. So, this looks similar to that of the 5 transistor one stage opamp as well as a telescopic, but please note because there are extra bias currents in the circuit you have to be a little bit careful when designing this particular opamp for slew rate.

Finally, we need to look at the noise and the mismatch. So, let us quickly look at noise as you might imagine we are just going to write down the expression for noise because we have studied what happens in the single handed folded-cascode. So, we should I did not know what happens when you convert it into a differential structure. So, we should now be able to write down the expression. So, you now have 11 sources of noise because you have 11 transistors. So, let us quickly write down each one. So, let us look at them in turn M 0 noise of M 0 splits between the 2 parts equally and therefore, appears as common mode noise at the output and gets cancel.

So, there will be no noise current flowing through the output. As always you can either look at the short circuit the output and look at the output noise short circuit current and divide by the transconductance of the opamp or you could look at it at no load condition and look at the divided by the voltage gain to get the input referred noise voltage. Either one of these will give you the same, same answer. So, noise of M 0 goes through identical paths especially at low frequencies and therefore, gets cancelled you assume that the 2 paths are identical. What about M 1 and M 2? Of course, the noise of M 1 and M 2 follow the exact same path as the signal and do appear at the output, and similarly

noise of M 9 and M 10 do appear at the output. What about noise of M 3 and M 4? At low frequencies they do not produce noise.

I again point out that this is true at low frequencies, at high frequencies because you have parasitic capacitances at the different nodes the noise from the cascode transistors can appear at the output. So, I will leave that as an exercise as a homework exercise for you to look at for a simple single ended cascade. You can also look at folded-cascode or a regular cascode for both of these transistors you will see the same effect at high frequencies.

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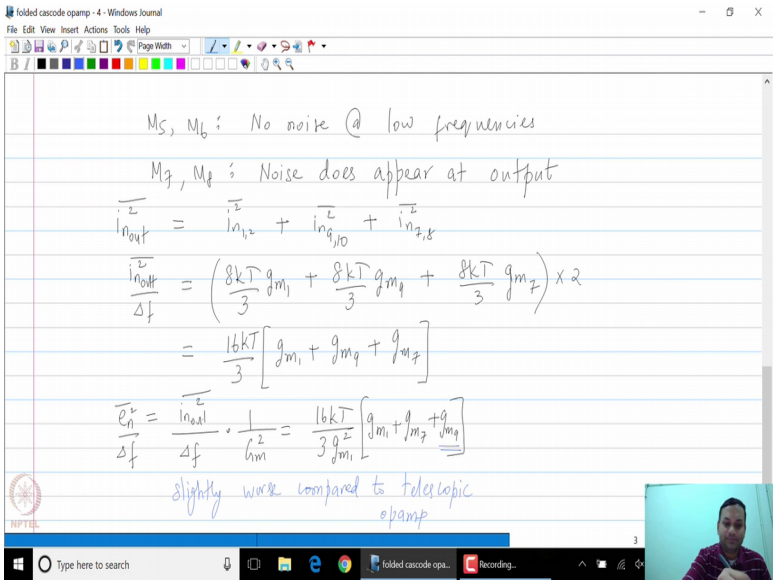

Similarly, transistors M 5 and M 6 will not have any noise at low frequencies because these are cascode devices and M 7 and M 8 will produce noise therefore, you will find that the output short circuit current will consist of 3 portions. So, you will see i n 1 and 2 plus i n 9 and 10 plus i n 7 and 8. And clearly these noise sources will not be correlated each one of them produces independent noise and therefore, the output referred noise thermal noise density will be 8 kT by 3 g m 1 plus 8 kT by 3 g m 9 plus g m 7 times 2. Because you have M 1 and M 2 M 9 and M 10 and M 7 and M 8. So, this noise is 16 kT by 3 into g m 1 plus g m 9 plus g m 7.

Again a reminder that as far as noise is concerned the drain noise is not injected symmetrically into the input into a any of these nodes you cannot use differential mode analysis to solve for noise I am just pointing that out there. So, the input referred noise

density would be e n squared over delta f would be divided by the square of the transconductance. So, this is clearly 16 kT by 3 g m 1 squared into g m 1 plus g m 7 plus g m 9. So, this is the input referred noise of the folded-cascode opamp.

Now, I want you to compare this to the telescopic opamp and you will find that there is an additional source of noise from the PMOS transistors M 9 and M 10 therefore, you expect the input referred noise, the noise performance of the folded-cascode opamp to be slightly worse compared to the telescopic opamp. This is because of the additional current sources M 9 and M 10.

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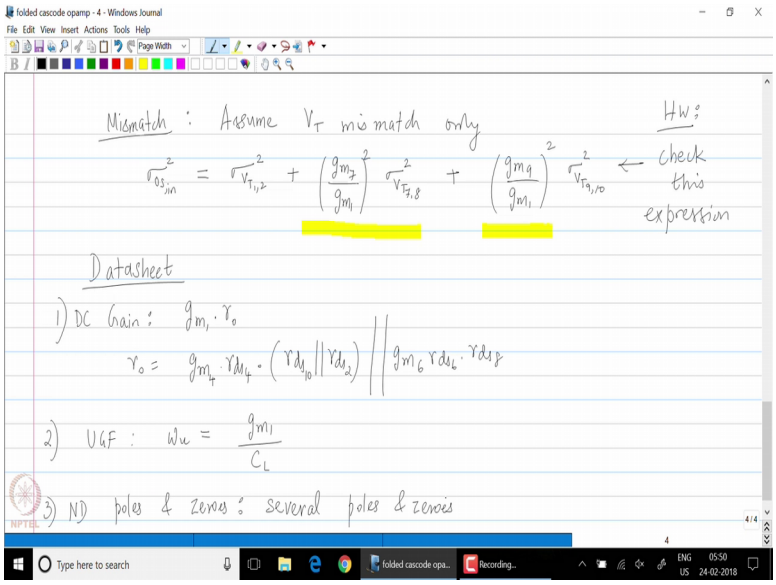

Similarly, if you were to look at mismatch we are going to assume only V T mismatch exists and you are trying to find out the input referred V T mismatch. So, as you might expect the mismatch of transistors M 1 and M 2 would appear directly at the input of the folded-cascode opamp. So, the expression for the input referred offset sigma squared o s in is going to consist of several different expressions the it could consists of the input referred offset of M 1 and M 2 appearing directly. And you will have 2 more expressions as you might imagine the mismatch between cascode transistors M 3 M 4 and M 5 M 6 do not appear at as an input referred offset at the input we have seen this effect before and even for the telescopic opamp and therefore, the other expressions you will get will now depend on V T 7 and 8 and 9 and 10.

As you remember as you might imagine the V T mismatch between M 7 and M 8 looks very similar to that of a telescopic opamp case and will be scaled by the ratio of the g ms of M 7 and M 1. So, that is the case for this transistor and these 2 transistors and finally, for M 9 and M 10 again there offset voltages are expected to be scaled by the relative ratios of g m 9 and g m 1 the whole squared. Now, we have simply written this down I want you folks to go ahead and figure out check if this is check this expression. I have just written it down based on intuition you need to figure out whether this intuition is correct or wrong. In other words whether V T 7 and V T 8 will appear as scaled by g m 7 over g m 1 whole squared and whether V T 9 and V T 10 will also be scaled by g m 9 over g m 1 the whole square. So, this is going to be a general homework exercise for all of you.

Now, we are in a position to write down the datasheet of the opamp. So, so we are able to compile the different expressions we will follow the same set of expressions as we have derived so far. So, the first thing you want to know about the opamp is the DC gain or the low frequency gain that is clearly going to be g m 1 times r o and r o is clearly you have 2 portions. So, the first portion is r up which is g m 4, r ds 4, times r ds 9 parallel r ds 2 in parallel with so that is the path looking upwards. So, you have g m 4 r ds 4 times the impedance looking upwards which is r ds 10 in parallel with r ds 2 and r ds 9 is the same as radius 10.

And looking down you have g m 6 r ds 6 times r ds 8 and as we have seen this is slightly lower than that of the telescopic opamp by an order of 2 or 3 times. The next parameter is the unity gain frequency omega u this is simply going to be g m 1 over C L, where C L is the load capacitance at the output node it is the sum of these actually the load capacitance and the parasitic capacitances. And the third expression is the expression for the non dominant poles and 0s as we have seen this opamp is going to have several non dominant poles and 0s for example, if I look at the path the signal takes from M 1. So, that signal goes through node x node, this node, this node, this node and this node. So, clearly you are going to see at least 5 poles for this particular circuit.

So, you are going to have several poles and 0s and as I mentioned this is a homework problem for you to analyze as to see how many poles and how many 0s you have from this particular opamp.

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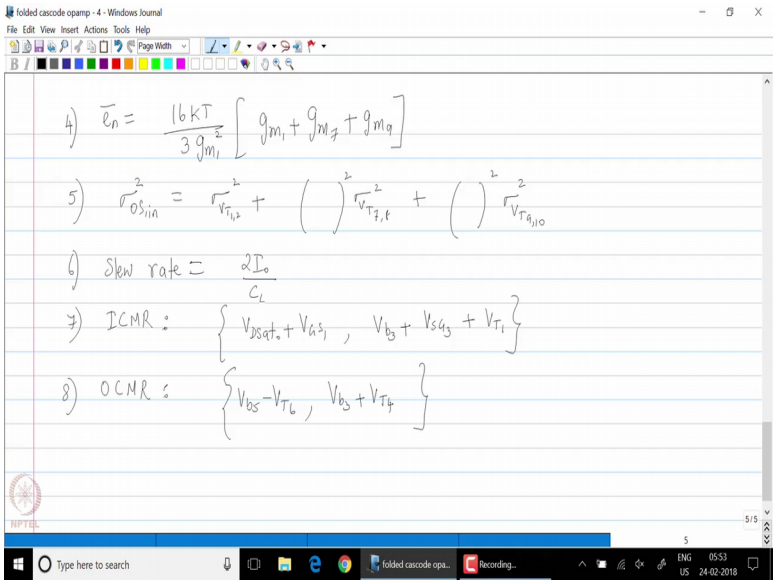

The 4th expression is going to be the input referred noise which we have just calculated. The input referred noise of the opamp is going to be 16 kT by 3 g m 1 squared into g m 1 plus g m 7 plus g m 9. As I pointed out before this is going to be slightly worse than the telescopic than that for the telescopic opamp and the input referred offset is going to consist of the offset of V T 1 and 2 directly appearing at the output and you have scaled versions of V T 7 and 8 and V T 9 and 10.

The next parameter that we need to look at is this slew rate. As we have seen for this particular opamp the slew rate is going to be 2 I naught over C L the input common mode range we have seen this the input common mode range is decided by when M 0 goes into triode and when M 1 goes into triode. So, as the voltage keeps decreasing M 0 will eventually hit the triode region when the input common mode range is V D sat 0 V d sat 0 plus V G S 1 and as the common mode input common mode increases so what will happen is that V x is constant at V b 3 plus V S G 3 and the input can go one threshold voltage above that particular voltage. So, that does nothing, but V b 3 plus V S G 3 plus V T 1.

So, the maximum voltage at the input can be V b 3 plus V S G 3 plus V T plus V T in bar. The output common mode range is of course, depends on, the output common mode range of course, depends on the values of V b 5 and V b 3 the minimum value occurs when M 6 hits the edge of the triode region and that can happen when the input voltage

goes 1 V T 6 below V b 5. And if the common output common mode increases that will cause M 4 to go closer to the triode region and that can happen at a voltage V b 3 plus V T 4.