Analog Integrated Circuit
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Lecture - 34
Folded-Cascode OpAmp-3

We are now in a position to build the full structure of the folded Cascode opamp. So, let us quickly do that the first thing we start off with is the input stage.

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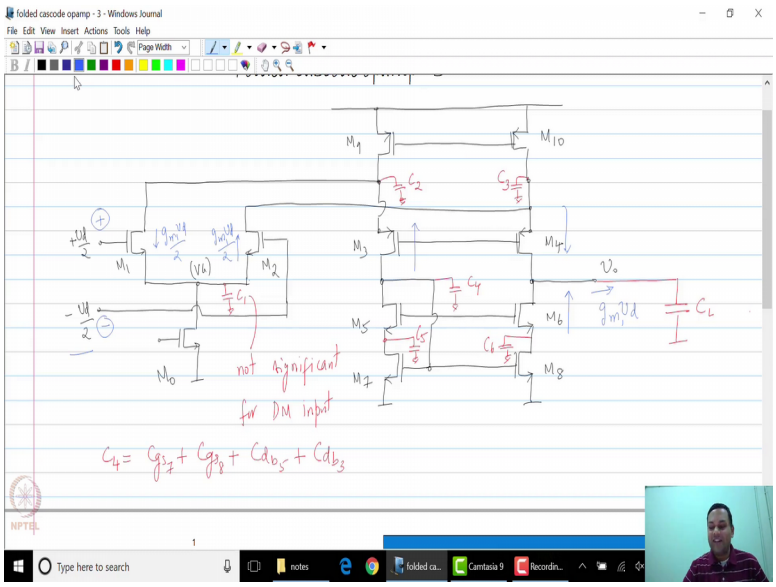

From the common source n mos, we will draw the n mos common source followed by the p mos common gate of folded structure and the input stage in the single ended version was a common source n mos transistor, when you move to a differential amplifier type of structure, the 2 transistors will be joint together to form a differential pair as shown here. So, this is your this is your n mos differential pair the inputs are plus Vd by 2 minus Vd by 2 and you have a current source at the bottom which some current source you know through some transistor M 0, let us say and the input transistor are M 1 and M 2, remember that in the single ended structure, they should go to a node which splits between the common gate p mos structure which is folded downwards and a current source at the top.

So, if I have to show the current source at the top the current source at the top would be replaced by p mos transistors. So, and at this node you have the splitting of the current

between the 2 parts. So, let us say that transistor M 1 is connected. So, and transistor M 2 is connected to this transistor this p mos transistor and finally, at this point the output goes into the common gate p mos structure this is the common gate p mos structure and this is the output remember now you need to con you need to get a single ended output and you need to get a current source at the bottom and therefore, this portion of the circuit will actually have a current mirror in this particular case this will be an n mos current mirror structure and because we want high swing from this particular structure we will use the high swing Cascode for the n mos current mirror and the output is correspondingly taken at this node.

So, let now mark the numbers of the other transistors. So, M 3, M 4 form the common gate structure in the single path and M 5, M 6, M 7 and M 8 form the current mirror at bottom and M 9 and M 10 form the current source at the top. Now, what about the let us quickly check the plus and minus signs of the opmap, we are drawn are correct.

So, if you were to apply a positive Vd by 2 at the gate of M 1 you expect this current to be positive and this current to be negative in this direction. So, this current would be pulled out from this node and through M 5 and M 7 and this would cause a corresponding a current to flow through M 6 and M 8 and if you look at this path there will be a current flowed from M 2 which will flow directly into M 4 and some of these 2 currents will slopes through the output. So, clearly the plus and minus signs of the opamp are shown.

Now let us now that we have drawn this basic structure of the opamp, let us quickly do the small signal analysis and try to come up with the expressions of the gain etcetera of the opamp.

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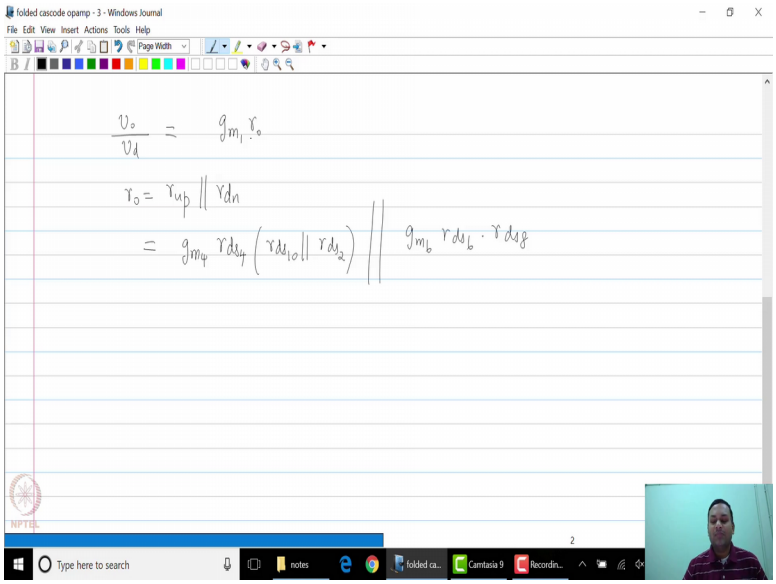

So, let us start off with the small signal gain of the opamp. So, we want the dc gain of the opamp if you were to look at the dc gain, you can see that the current through M 1 and M 2 because this is a differential pair with this node being a virtual ground the current through M 1 would be gm times Vd by 2 flowing downwards the current through M 2 would be gm times Vd by 2 flowing upwards because a minus Vd by 2 voltage is applied at it is gate and we are also going to assume that the transistors are designed such that most of this current does not flow through M 9 and M 10, but flows down into M 3 and M 4 and therefore, the total current going out would be gm times gm 1 times Vd.

Now, where does this current flow this current flows through the total output impedance at you know at the output node for the dc gain, we will assume that there is no node or if there exists any node it is a capacity node and let us quickly calculate the expression for the r out. So, r out has 2 components an upward looking resistance and the downward looking resistance the upward looking resistance is nothing, but gm 4 rds, 4 times the rds of M 10 in parallel with the rds of M 2; this is the impedance looking upwards and that comes in parallel with the impedance looking downwards which is gm 6, rds 6 times rds 8. So, this is overall output resistance.

Clearly then Vo mins Vo by Vd needs to be gm 1 times ro and as we have pointed out before this is quite large this is only a little bit smaller than the than the may be than the

square of the intrinsic gain of a transistor. So, this is the small signal gain of the of the folded Cascode opamp.

Now, that we had found out the small signal gain we should also write down the expression for the frequency response of the small of the folded Cascode amplifier. So, now, let us assume I am going to show that in red let us assume that there are capacitances at every node of the circuit. So, you have capacitance at this node and infact every node of the circuit and let us assume that you also have some node capacitance at the output and so, at the output node you have CL plus you know some parasitic capacitances as you can see you now have large number of capacitances n the circuit very similar to the telescopic opamp what do these capacitances consists of; so, for example, let me number these capacitances c 6 six capacitances and let us assume that CL consists of the node capacitances plus all other capacitances.

For example capacitance c one will not be significant for differential mode analysis this is because the common mode of source M 1 and M 2 is going to be a virtual ground is going to be a small signal ground for a differential input what about capacitance at let us say note four. So, let us say c 4. So, c 4 for example, would consists of capacitances gate source capacitance of M 7 plus gate source capacitance of M 8 plus the drain bulk capacitance of M 5. So, you can see there is capacitance from M 7 capacitance from M 8 capacitance from M 5 and of course, drain bulk capacitance from M 3, this is an example each one of these capacitances will have contributions from the respected transistors connected to that particular node.

What do we know about the frequency response the frequency response will have a certain number of poles and 0s and the number of poles and 0s will depend on the number of nodes that the signal passes through the number of poles would depend on the number of nodes that the signal passes through the number of 0s would depend on whether there is a phase shift through the different parts clearly in this case you do expect a phase shift.

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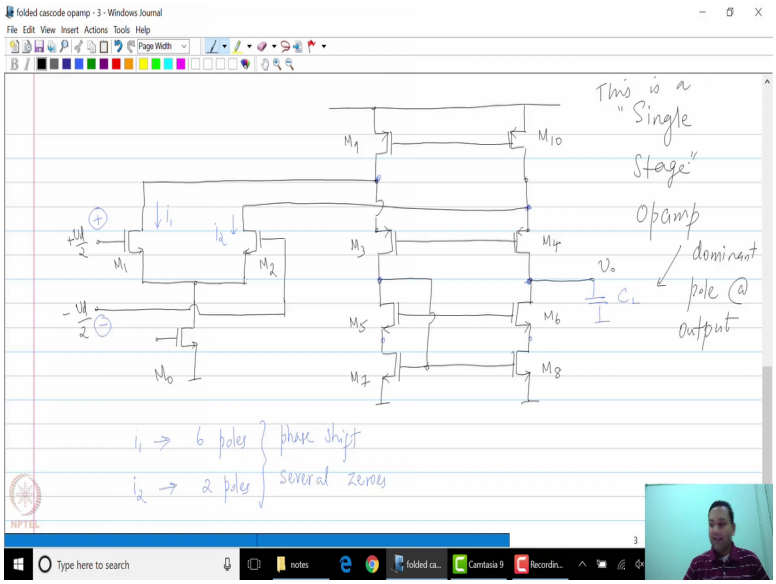

Because if you look at the current through M 1 for example, though maybe; we can draw that on a different page if you look at the current through M one. So, the current through M 1 passes through this node. So, let us say that is node one sorry I do not want to name the nodes. So, that passes through this node. So, you will get a pole from that it passes through this node you get a pole here it passes through this node it passes through this node and finally, at the output.

So, clearly you expect; i 1 to pass through this 5 nodes. So, we expect and of course, the output node. So, you expect 6 poles in the no expression for i 1 over v out over i 1 and if you look at i 2; i 2 of course, passes through this node and at the output node and as you can see i 2 only has 2 poles and now these 2 currents gets summed at the output you can clearly see that there is a phase shift between the 2 parts you too expect you do expect 0s in the transfer function and now because there are there is a large difference between the number of poles in the 2 parts you expect several 0s in the transfer function.

Now, 2 things first of all I would encourage you to think about the number 0s and number of poles that you can get out of the circuit if you show desire for your benefit it might be useful to quickly do this small signal analysis assuming a capacitance at every node that will give you some insight the analysis is expected to give you some insight as to the number of poles in each part and when you add the 2 currents you will also be able

to see the formation of the 0s and it is also give you insight as to the number of 0s that you would expect from this particular structure.

Number 2 we also want to know what is the dominant pole in this particular structure and as you might expect you thi you should expect that the largest capacitance comes from the node capacitance because in some sense this is still a single stage opamp. So, this is still a single stage opamp because this is the dominant pole the output pole is the dominant pole.

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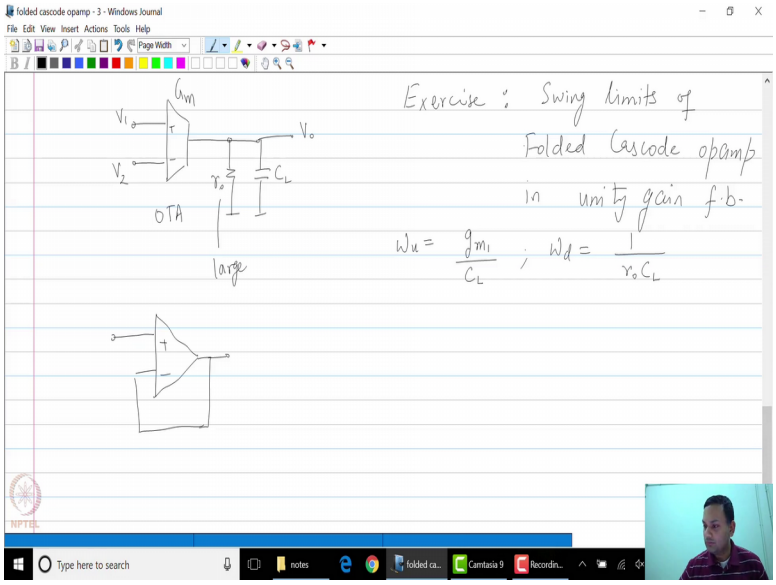

So, you still expect this to be a single stage opamp and in other words, if you were to draw the equivalent circuit for this particular circuit for this particular opamp it will look like an operational trans-conductance amplifier with a certain output impedance and a certain capacitance. So, this is ro and you have CL and it has a certain trans-conductance. So, if you were to look at the overall output you are basically trying to create you started from a one stage opamp which had a simple trans conductor you went to the telescopic opamp which had which look like a better trans conductor and now you have a folded Cascode which still looks like a very good trans conductor much better than the regular original one stage opamp because r out is large, but the swing limits are expected to be better than that of a telescopic opamp.

So, I would encourage you to as an exercise I want you to think about the swing limits of the of the folded Cascode opamp in unit gain feedback. So, you need to convince

yourself that the same problem that you had with the telescopic opamp where you had a swing limit limitation when you connected the opamp to unity gain fee back does not exist for the folded Cascode opamp, I will just remind you that from the basic structure this is just a quick hint that the input common mode is now somewhat isolated from the output common mode in this particular structure. So, you should apply the unity gain feedback on this particular structure and convince yourself that it really does not have the same problem.

What about the coming back to the frequency response. So, the in such a structure you expect it to be a very good integrator you expect the unity gain frequency to be dominated by the dominant pole and clearly that should be gm one over CL the of course, the dominant pole omega d should be at 1 over r out CL because this particular opamp has a much larger output resistance it will have a much smaller dominant pole compared to a compared to a regular 5 transistor one stage opamp which we studied right at the beginning even before the telescopic opamp .

So, we are now in a position to also look at the input and output common mode ranges of the particular telescopic opamp. So, let us first look at the input common mode range.

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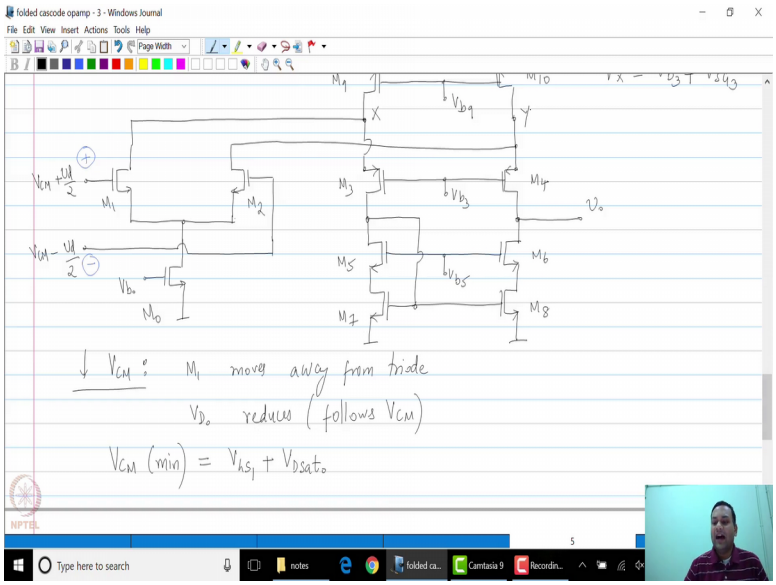

We will now assume that the input common mode as VCM, let us say that I should apologise I should add the bias voltages at this nodes because they are not let hanging you have to have a bias voltage I will call them Vb 9 and Vb 5 and Vb 0. So, there are 4

voltages that need to be applied to the folded Cascode opamp Vb 0 for M 0 Vb 9 for M 9 Vb 3 for M 3 and Vb 5 for M 5. So, for completeness sake let me make sure that the voltages are added here also.

So, now we are in a position to study the study the input and output common mode ranges of the of the folded Cascode opamp. So, let us now assume that the input common mode starts to drop. So, let us say decrease VCM what is the common mode at node x for example; so, clearly the common mode at node x. So, I call that Vx; Vx has to be Vb 3 plus VSG 3. So, the common mode at node x is fixed relatively fixed because Vb 3 is fixed and the currents in the transistors are assumed to be fixed therefore, if you start decreasing VCM all the other transistors will are expected to be remain in saturation till some transistor goes into triode cut off.

Now, as you can see in this case Vx stays constant, but VCM is decreasing M 1 moves away from triode, but it carries the same current therefore, what will happen the drain node of M 0? So, I will call that Vd 0 reduces and it follows VCM with a difference of VGS 1.

So, when you try to reduce VCM the input common mode voltage Vd 0 reduces which is the drain voltage of M 0. So, M 0 clearly goes towards the triode region. So, the minimum value of VCM is equal to VGS one plus Vd sat 0. So, this is the minimum value beyond this M 0 goes into triode region.

Now, what happens if you start increasing VCM this will give you the maximum limit clearly that will happen when M 1 goes into triode M 1 or M 2 that is because nodes x and y are held constant at Vb 3 plus VSG 3 therefore, the gate voltage of M 1 is increasing the drain voltage is constant.

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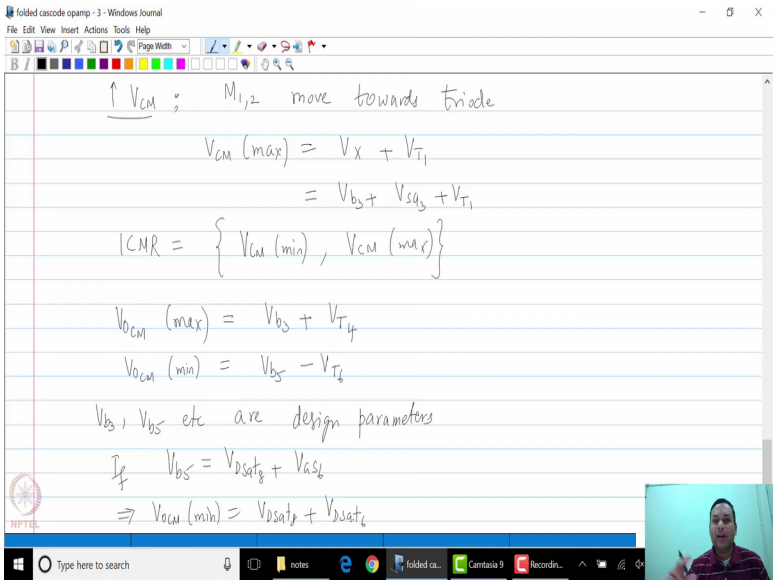

So, clearly it is moving towards triode region and VCM max will be given when the transistor M 1 and M 2 goes hits exactly hits the edge of triode region and that can happen when the gate raises to 1 threshold voltage above the drain voltage. So, the maximum voltage is Vx plus Vt 1; Vx is clearly Vb 3 plus VSG 3 plus Vt 1. So, the reminder node x is an Vb 3 plus VSG 3 and the gate voltage can raise one threshold voltage above that before M 1 and M 2 hits the edge of the triode region.

So, this is the maximum value of VCM. So, therefore, the input common mode range is the; this over all range of VCM min to VCM max this is the input common mode range of the; what about the output common mode range. So, now, let us find out what is the; what are the maximum and minimum voltages that can be achieved at the output the maximum voltage that can be achieved at the output. So, the VoCM, if the output voltage starts increasing you can see that the gate of M 4 is constant which is db 3 and the drain voltage can raise one thresh hold voltage above the gate and for the p mos transistor.

So, therefore, Vb 3 plus Vt 4, this has been maximum voltage that the drain of the p mos can achieve VoCM min. Similarly, it is determined when the n mos transistor M 6 hits the edge of triode region gate of M 6 is held constant at v five, but the drain is being lower, it can swing 1 Vt below the gate. So, the minimum value is Vb 5 minus Vt 6.

Now, please note that Vb 3 and Vb 5 themselves all the bias voltages are under the designers control. So, for example, Vb 5 can be as low as Vd sat 8 plus VSG plus 6. So,

clearly these 2 are may all these bias voltages are designed parameters for example, you could design current mirror consisting of M 5, M 6, M 7, M 8 to be biased such that the output can go as low as this. So, Vb 5 if Vb 5 were equal to Vd sat 8 plus VGS 6, if this were the case, then you can see that you can see that vocm minimum is now equal to Vd sat 8 plus Vd sat six. So, clearly VoCM may; can be very low as long as the bias voltages are chosen appropriately.

Similarly, VoCM max can be as high as Vd d minus minus Vd sat 10 minus Vd sat 4. So, let us just quickly write that down here so.

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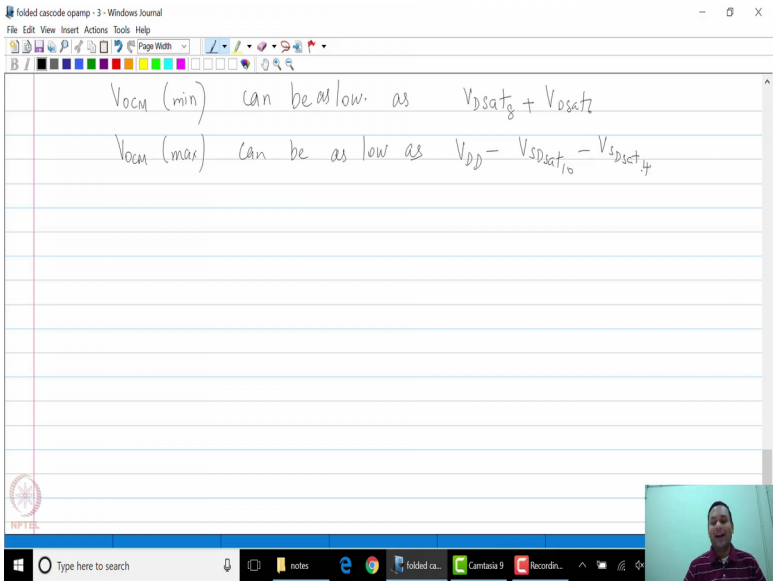

So, if design properly I say can be low, but what this means is that you need to choose Vb 3 and Vb 5 etcetera carefully I am just simply writing it as; since I am writing it as sum of 2 Vd sat I can just write it as 2 Vd sat in other words it is Vd sat 8 plus Vd sat 6 and similarly vocm max can be as low as VDD minus VDD minus Vd sat 10 minus Vd sat four. So, the swing limits are can be designed to be moderately high this is still of course, not as high as the regular you know 5 transistor one stage opamp that we initially studied, but it is definitely you know you know it can be designed to have certain moderate values and now, let us look at the other parameter of this opamp, we have looked at the input common mode range we have looked at the output common mode range and we have looked at the we have looked at the gain and we have looked at the

frequency response. So, the other 2 parameter we are interested in are the; are the noise and outset of the folded Cascode opamp.