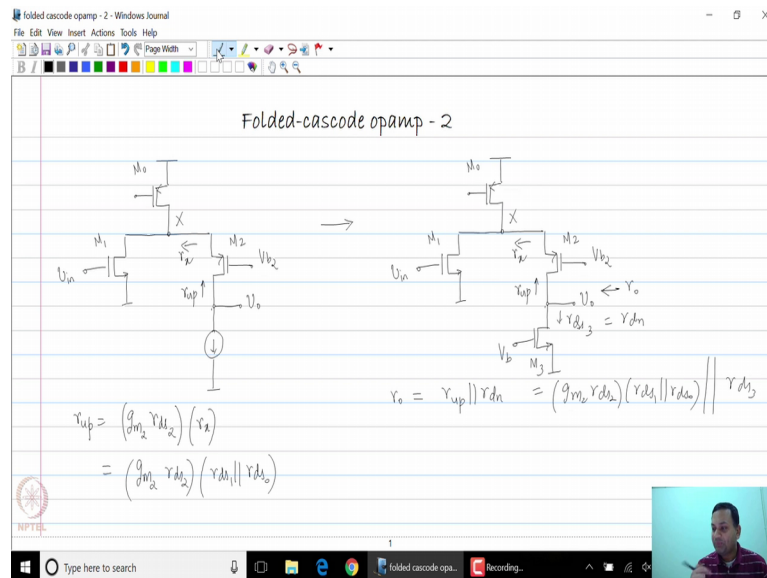


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Lecture – 33
Folded- Cascode OpAmp – 2

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Before we build the full opamp using the folded cascode structure let us take a look at the gain and noise performance of the simple single ended folder cascode structure. So, we will assume that the input is an NMOS anti cascode is a PMOS a device.

Now, we need to do something about the output mode. Now, earlier we had look for simplicities case we have assumed that the output is resistively loaded, but it normally does not make sense because the minute you have a resistive load you really do not need the large output impedance that this particular structure offers right. So, you really want to get high DC gain from the structure. So, naturally you ideally want to use an ideal current source so that you will get the gain of maximum you will get the advantage of maximum gain from this particular opamp.

Now, how do you get up how do you make a current source you of course, cannot make ideal current sources in practice. So, the first thing you try to do is to try to replace that with a transistor. So, please note that the output impedance of this, so maybe I will call that r up, r up is something we need to write down. So, before we you move want to the

replacing the current source because this is going to become significant in a few minutes. So, what is the expression for r_{up} . So, as you can see the gate of M_2 is connected to a constant voltage and therefore, M_2 is a common gate structure. You know that any impedance at the source of the common gate structure is multiplied up by the intrinsic gain of the common gate transistor. So, therefore, you expect the impedance to be $g_{m2} r_{ds2}$ times r_x if this node was node x times r_x and this is $g_{m2} r_{ds2}$ times r_x is of course, the parallel combination of I_{D1} parallel r_{ds0} .

So, this is the impedance looking upwards at the drain of M_2 . So, this is of course, quite high we. Now, want to use an ideal current source here, but we know we cannot do that. So, let us first try to replace that with transistor with an NMOS transistor because this is a current flowing downwards. So, the first thing we will try to do is to replace it with some V_b that it is gate such that this has some correct. Now, clearly this NMOS transistor will now, have some resistance let us say, let me call this M_3 this will have some resistance r_{ds3} and therefore, r_{down} will be equal to r_{ds3} and the total resistance at the output which is the output resistance r_o is r_{up} parallel r_{down} and this is clearly, this is clearly the parallel combination of $g_{m2} r_{ds2}$ into r_{ds1} parallel r_{ds0} in parallel with r_{ds3} . And now, we can see that the impedance looking upwards is of the order of $g_m r_{ds}$ square it is slightly lower than $g_m r_{ds}$ square whereas, the impedance looking downwards is just of the order of r_{ds} .

It is going to be very different to make a very difficult to make these of the same order and typically what you will find is that r_{down} in such a case will always be how much smaller compared to r_{up} . This is not the best case because you wanted up current source which would have much higher impedance compared to the impedance looking upwards which will give you the maximum gain from this particular stage. So, now it becomes clear to us that you need better current source at the bottom.

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$r_{dn} = (g_{m3} r_{ds3}) \cdot r_{ds4}$
 $r_o = r_{up} \parallel r_{dn}$
 $= g_{m2} r_{ds2} (r_{ds1} \parallel r_{ds3}) \parallel g_{m3} r_{ds3} r_{ds4}$

→ in general, gain & r_{out} of folded cascode are 2-3 times smaller than regular cascode.

$i = g_{m1} v_{in}$
 $i = i_1 + i_2 \text{ (KCL @ X)}$
 Assume $r_{ds2} \ll r_{ds1} \text{ \& } r_{ds3}$

So, now, if you want the better current source you of course, have to use a cascode structure even at the bottom. This will give you an even better output resistance. So, let me call these transistors M 3 and M 4 with gate voltages V b 3 and V b 4. Now, if you use this current source r_{down} will be equal to $g_{m3} r_{ds3}$ times r_{ds4} and therefore, you are overall output resistance which is r_{up} parallel r_{down} will become equal to $g_{m2} r_{ds2}$ times r_{ds1} parallel r_{ds0} in parallel with $g_{m3} r_{ds3}$ times r_{ds4} .

Now, as you can see this is somewhat close to that of the telescopic cascode, but you just note that because of this particular terms here this gain would be slightly smaller and in general gain and r_{out} of the folder cascode. So, will be around to 3 time smaller then the telescopic version which is the regular cascode (Refer Time: 07:15). So, in general now, when you try to decide all of these r_{ds} values you will find that it is a little bit lower than that of the regular cascode, but it is still much higher than that of the regular one stage opamp this is simple common source structure. But, so this is the template that we are going to use for our analysis. So, this is the 5 transistor structure for the folded cascode single stage, folded cascode single ended folded cascode. So, now we can write the expression for the gain. So, let us assume that a voltage V_{in} is applied to the gate of M 1 clearly that should also include some bias voltage V b 1 the bias voltage at a gate of M 0 should be V b 0.

Now, let us look at what will happen when you apply a signal I am not going to draw the small signal structure because we have now, at a point where we should be able to visualize the small signal structure of each circuit and of slightly more complicated subjects. So, when I apply this V_{in} between the gate source of M_1 you will have a current I_1 flowing through M_1 I_1 should clearly V_{gs1} times V_{in} and this I_1 has 2 paths to flow the first path is through transistor M_0 the second path is through transistor M_2 and of course, with the opposite direction since I have already chosen the direction. So, these will be the 2 directions of I_1 . So, I_1 should be equal to I_3 sorry I_0 plus I_2 and this is purely from KCL are known x.

Now, part of this correct will of course, flow through M_0 ideally you want to design the circuit such that as much of I_1 flows into M_2 as possible. What is the impedance of the circuit looking downwards at the source of M_2 ? Please note that the impedance at the drain of M_2 is quite large. So, you cannot assume that the input impedance at, you cannot assume that the input impedance at the source of M_2 is equal to $1/g_m$. So, this particular assumption is not valid because you have actually connected a very large resistance at the drain of M_2 . So, please note that.

So, the current will split and some form depending on the 2 impedances. Now, this current will now flow through the output node at V_0 the total output impedance is given by r_{out} and therefore, that will give you a certain amount of gain. So, this will give you the small signal gain. So, I will let us assume that we design M_0 such that it has much higher impedance compared to the output impedance of r_{ds} of M_1 and the input impedance is the source of M_2 .

So, I am going to call that r_{s2} . So, that will distinguish it. So, we will assume that r_{s2} is designed to be smaller let us say much smaller than r_{ds1} and r_{ds0} . So, there are 3 paths for the current to flow at node x, one of them is the output impedance of transistor M_1 the other is the output impedance of transistor M_0 and the third path is through the you know source of M_2 itself.

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$$V_o = -i_1 \cdot r_{out} = -g_{m1} r_{out} \cdot V_{in}$$

$$\frac{V_o}{V_{in}} = -g_{m1} r_{out} = -g_{m1} \left[\left\{ g_{m2} r_{ds2} (r_{ds1} \parallel r_{ds0}) \right\} \parallel \left\{ g_{m3} r_{ds3} r_{ds4} \right\} \right]$$

Noise
 $M_1: \bar{i}_{out1} = \bar{i}_{n1}$
 $M_2: \bar{i}_{out2} = \bar{i}_{n2}$
 $M_3: \bar{i}_{out3} = -\bar{i}_{n3} + \bar{i}_{n4} = 0$

So, we will assume this is true and therefore, the small signal gain V_{in} , we now assume that all of I_1 the circuit has been designed such that all of I_1 close to M_2 . So, the small signal gain now, is minus I_1 times r_{out} sorry this is the output voltage is minus I_1 times r_{out} . So, this is minus $g_{m1} r_{out}$ times V_{in} . So, V_o by the V_{in} which is the small signal gain of the circuit which is minus g_{m1} times r_{out} . So, this is minus g_{m1} times as we have seen r_{out} as $g_{m2} r_{ds2}$ into r_{ds1} parallel r_{ds0} in parallel with $g_{m3} r_{ds3} r_{ds4}$.

So, this is the expression for the small signal gain of this particular folded cascode structure and this will give you slightly lesser gain compared to the regular cascode, but this is still larger than the simple common source structure value would have seen before.

So, now let us look at a noise performance of this particular cascode structure. So, let us first make a copy of this particular amplifier so that we can now, analyze it for noise. So, as always when you analyze for noise the first steps are to apply the appropriate voltage and current conditions in the circuit. So, clearly when you are doing analyzing for noise that you assume there is no input signal because the noise is uncorrelated with the signal. So, therefore, there is no input signal and since noise is a small signal quantity you assume that small signal equivalent circuits are valid and therefore, the bias voltages at the appropriate nodes will be grounded.

And so far so good. So, now this structure you find that there are actually 5 sources of noise in this circuit and the 5 sources of noise are the drain current noise, i_{n1} of M_1 , i_{n0} of M_2 , i_{n0}^2 of M_0 , i_{n2}^2 of M_2 , i_{n3}^2 of M_3 and they will all be squared of M_4 . So, there are clearly 5 different sources of noise in this particular circuit. Now, let us look at each one of these and figure out if that noise will make its output.

The easiest way we have seen earlier is to short the output to the ground and then look at the output short circuit noise current. So, in short circuit condition we are going to look at the output noise we will of course, assume that the noise of each transistor is uncorrelated with each other. And now, we need to find out the mean squared sum at the output now; let us start going to each of these M_1 by 1 . So, this is noise analysis. So, if you look at noise of M_1 . So, you will find that the noise of M_1 and you do this noise of M_1 we will assume that the other noise forces do not exist and this noise of M_1 flows between the drain and source of M_1 .

So, at node x this current has 3 parts of 3 ways to split it can split just like your small signal, it can split through r_{ds1} , it can split through r_{ds0} and it can split through the source resistance seen the resistance seen looking into the source of M_2 .

As we have seen earlier just right here we have assumed that we have assumed that r_{s2} is much smaller than r_{ds1} and r_{ds0} so that most of the current flows through M_2 to the output. And clearly since we have designed a circuit such that that happens for the signal you should expect that all of i_n 's one squared appears at the output. So, the first component of $i_{n,out}^2$ which is $i_{n,out1}^2$ is equal to i_{n1}^2 . So, pretty much all of noise of M_1 will appear at the output short circuit. What about M_2 ? If you look at noise from M_2 , if you look at the noise of M_2 that is again a current source which is across the drain source of M_0 sorry noise of M_0 it is across the drain source of M_0 and as you can see from usually from the circuit topology this looks yeah you know i_{n0} looks exactly the same as i_{n1}^2 purely from a circuit topology.

You should expect that i_{n0}^2 also has 3 paths to flow through the first one is through r_{ds1} , the second one is through r_{ds0} and the third path is the impedance looking in at the source of M_2 . So, therefore, you should expect that $i_{n,out2}^2$ should be equal sorry $i_{n,out0}^2$ should be equal to i_{n0}^2 this is the second component of noise.

What about M_2 ? Noise from M_2 , so M_2 remember is the common gate structure normally you do not expect additional noise from M_2 because as you might expect the noise from the cascode does not make its way to the output. Let us confirm that this is indeed true by doing the following. So, let us consider the noise from M_2 . Now, we do not know how to analyze this really well. So, when then current source is connected across 2 loads of the circuit. So, we go back to the earlier at the trick that we have studied earlier we will now, split this into 2 correlated the current sources.

So, just to remind you I will now, show that if you have will now, point out that if you have current source i between 2 nodes 1 and 2 as far as the rest of the network is concerned this is exactly the same as putting 2 current sources in series because the rest of the network assumes that current i is pulled out of node 1 and pushed into node 2 and KCL is clearly valid even at the intermediate. And this is again not changed if I were to connect this to any convenient voltage because there will be no current through this particular branch and I will connected conveniently to ground.

So, now how does this affect us? I can now replace this with a pack of current sources. Let us just each of value i_n and I connect this conveniently do not know. So, now this makes that job much easier because now, I can consider these 2 current sources. The only thing I have to keep in mind are that these 2 currents are correlated noise current sources. So, therefore, I cannot work with mean square values I have to work with the root mean square values and keep in track of the keep track of the sign.

So, now let me use 2 different colors to distinguish between these 2 guys. So, let me use red and blue if you look at noise correct i_n I expect that to behave exactly the same as noise current of M_0 and M_1 . I expect all of that current to go through M_2 into the output short circuit. And this should be clear because looking in at the source of M_2 I have a short circuit at the drain of M_2 and therefore, looking in impedance at the source of M_2 here would be $1/g_m$ in this case in the case of noise analysis and that is clearly much much smaller than r_{ds0} and r_{ds1} . And so clearly noise of all of i_n in blue color will flow into the output short circuit. So, the component, $i_{n,out2}$ I am still following the root mean square value will have a component being pulled out and I am going to call that $i_{n,2,1}$ and that is being pulled out.

What about the red color current source? So, that current source has 2 paths to travel one as looking down looking up at the drain of M₂, the other has through the short circuit clearly this current is again going to flow through this and so maybe I can just use directly $i_{n\ out\ 2}$ is going to be equal to minus $i_{n\ 2}$ plus 2. These are the directions of the 2 current sources in blue and red.

As you can see these 2 current sources are equal and opposite and therefore, this current is going to be 0. As you can see there is clearly no noise generated from M₂ at the output and therefore, this we have seen before even for the regular cascode when we analyze the noise for the telescopic opamp. You do not expect noise from the common gate structure especially at low frequencies.

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M_3 : No noise @ output
 M_4 : $\overline{i_{n\ out\ 4}} = \overline{i_{n\ 4}}$
 $\overline{i_{n\ out}} = \overline{i_{n\ out\ 0}} + \overline{i_{n\ out\ 1}} + \overline{i_{n\ out\ 2}} + \overline{i_{n\ out\ 3}} + \overline{i_{n\ out\ 4}}$
 $= \overline{i_{n\ 0}} + \overline{i_{n\ 1}} + \overline{i_{n\ 4}}$
 $\overline{e_n} = \frac{\overline{i_{n\ out}}}{g_m} = \frac{\overline{i_{n\ 0}} + \overline{i_{n\ 1}} + \overline{i_{n\ 4}}}{g_m^2}$
 $\frac{\overline{e_n}}{\Delta f} = \frac{8kT}{3} \frac{(g_{m_0} + g_{m_1} + g_{m_4})}{g_m^2}$

What about M₃? Transistor M₃ is again a common gate structure you do not expect any noise at the output you can follow the exact same procedure and show that the output noise generated by M₃ is equal.

And M₄ of course, will generate noise all of this noise will flow through the output. So, therefore, the total output short circuit noise which I will call by $i_{n\ out\ square}$ is going to be $i_{n\ out\ 0\ square}$ plus $i_{n\ out\ 1\ square}$ $i_{n\ 2\ square}$ remember I have 5 noise sources I need to calculate the effect of short circuit current and the root mean squared value for all 5 of them. So, these are the 5 components. We have already established that noise from M₂ and M₃ 0, so these two are 0 and therefore, for the cascode you have 3 sources of

noise. So, this is i_{n0} once, i_{n0}^2 plus i_{n1}^2 plus i_{n4}^2 I put this. So, there are these sources of noise this is the short circuit noise the input referred noise voltage which I will now, represent as e_n square is nothing, but the short circuit noise over the overall effect of trans conductance square. The effect of trans conductance of the circuit is of course, g_{m1} I will write the down here that is the g_m effect of trans conductance of the overall amplifier.

So, therefore, the input referred noise is going to be i_{n0}^2 , i_{n1}^2 plus i_{n4}^2 square over g_{m1}^2 and what is i_{n0} that is clearly $8kT$ by $3g_{m0}$ and let us say that I am interested in being that intensity and remember I am looking only at thermal noise I can always add the (Refer Time: 27:34) noise component of this as and when required.

So, this is clearly $8kT$ by 3 into g_{m0} as g_{m1} , g_{m4} over g_{m1}^2 . So, of course now, similar to the cascode you can see that you can look at the conditions that you would need to get a totally 2 noise solution you clearly need to maximize the value of g_{m1} and minimize the relative values of g_{m0} and g_{m4} . So, clearly the g_m of transistor 1 should be maximized the g_m 's of this transistor M_0 and M_4 should be minimized for you to achieve very low input referred noise.

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The image shows handwritten notes on a digital notepad. At the top, there is an equation for the output voltage:

$$\frac{V_o}{V_{in}} = -g_{m1} r_{out} = -g_{m1} \left[\left(g_{m2} r_{ds2} (r_{ds1} \parallel r_{ds0}) \right) \parallel \left\{ g_{m3} r_{ds3} r_{ds4} \right\} \right]$$

Below this, there is a circuit diagram of a folded cascode opamp. The circuit includes transistors $M_1, M_2, M_3, M_4, M_0,$ and M_{10} . Currents $i_{n0}, i_{n1}, i_{n2}, i_{n4}$ and voltages $v_{ds1}, v_{ds2}, v_{ds3}, v_{ds4}$ are labeled. The diagram is annotated with "Noise" and "Naive".

Next to the circuit diagram, there are several equations:

- $M_1 : i_{n_{out1}} = i_{n1}^2$
- $M_0 : i_{n_{out0}} = i_{n0}^2$
- $M_2 : i_{n_{out2}} = -i_{n2} + i_{n2} = 0$

At the bottom left, the overall transconductance is given as:

$$G_m = g_{m1}$$

The notepad interface includes a toolbar with drawing tools and a Windows taskbar at the bottom with a search bar and system tray icons.

Now, we are in a position to build the folded, full folded cascode opamp and write down directly its noise, noise expressions and gain expressions and so on. That is what we will do in the next lecture.