Analog Integrated Circuits
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Lecture – 32
Folded- Cascode OpAmp – I

In this lecture we are going to look at a new type of opamp called the Folded-cascode opamp.

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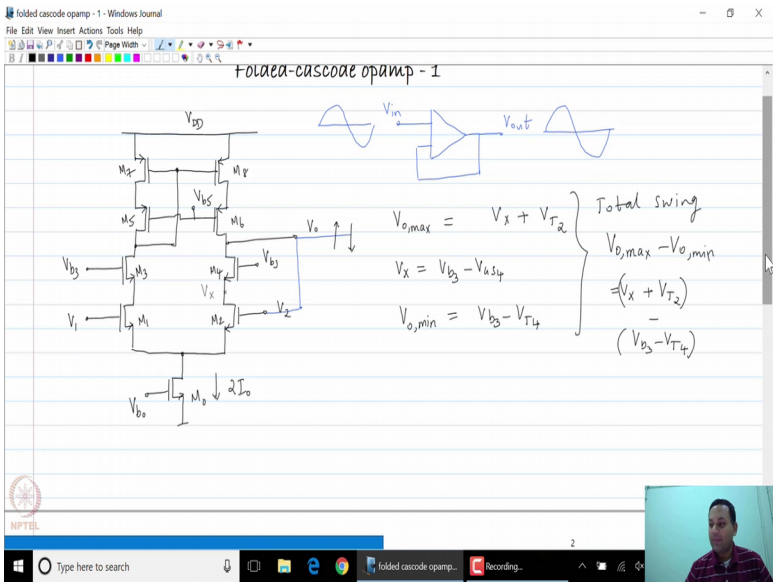

Before we do that let us first quickly see why we need a different kind of opamp. So, the cascode opamp seems to do most of the things that we want to do. So, let us quickly see if you know there are any drawbacks. So, let us quickly draw the structure of the folded-cascode opamp that we have been seen so far and use the NMOS version for illustration and let us say that the bias voltages are as shown. So, gate of M 0 gets a voltage V b 0, gate of M 3 and M 4 get voltages V b 3, gate of M 5 and M 6 get a bias voltage V b 5 and this is the output taken at the drain of M 4 and M 6 and V 1 and V 2 are the inputs. This is, are standard structure which we are saying for the further folded for the telescopic opamp.

Now, we want to see what the issue at this is. So, one of the most important issues can be seen if you apply unity gain feedback on this particular opamp. So, in other words I am building the opamp in this structure, I am trying to build a unity gain structure from this

opamp. So, I want V out to be equal to V in. So, I will have some DC value and on top of this I will have some certain swing and at the output I should get an exact replica for both DC and AC.

Now, let us look at what will happen in this case the first thing we need to see is whether the bias point is correct and it turns out that the bias point would be perfectly fine for this opamp. But the minute you apply the swing it turns out that there are some swing limit issues with this particular opamp, so to illustrate that I am going to call the voltage at this node V x. So, let us try to find out what are the maximum and minimum voltages at the output node in unity gain feedback condition. So, the maximum value, let us say V o is now starting to increase.

So, as V o starts increasing as you can see V x is that a constant voltage which is given by V b 3 minus V G S 4. So, V x is always at this constant voltage and of course, I am assuming that there is a total current 2 I naught, so that there is a current I naught each through M 1 M 2 M 3 M 4 etcetera and this is the value of V x. Now, the maximum value of V o is will occur when M 2 hits the triode region because as you can see the gate of M 2 stays almost constant at the x and the drain of M 2 stays almost constant at V x, but the gate keeps increasing. So, eventually this transistor M 2 will reach triode when M 2 goes into triode and that will happen when the gate becomes larger that the drain by a value of V T h 2, so V T 2. So, that will happen at this condition.

Now, what about the minimum value of the output voltage? So, now, let us say that the output is decreasing, so of course, M 2 goes further and further away from triode, but let us look at M 4 now. So, if you look at M 4 transistor M 4 you will see that its gate is constant at V b 3, but the drain voltage keeps dropping and; that means, that eventually M 4 will hit the edge of the triode region. Now, in that happens the condition on the voltages will be V o min the minimum value can hit one threshold voltage below V b 3 and that is given by V b 3 minus V T 4.

So, now we have found out the maximum and minimum values for the output voltage. This, these 2 voltages will determine these are the common mode over the ranges with the output with this condition and with this we will be able to figure out what the total swing allowable swing at the output is. So, V o max minus V o min and that is equal to V x plus V T 2 minus V b 3 minus V T 4.

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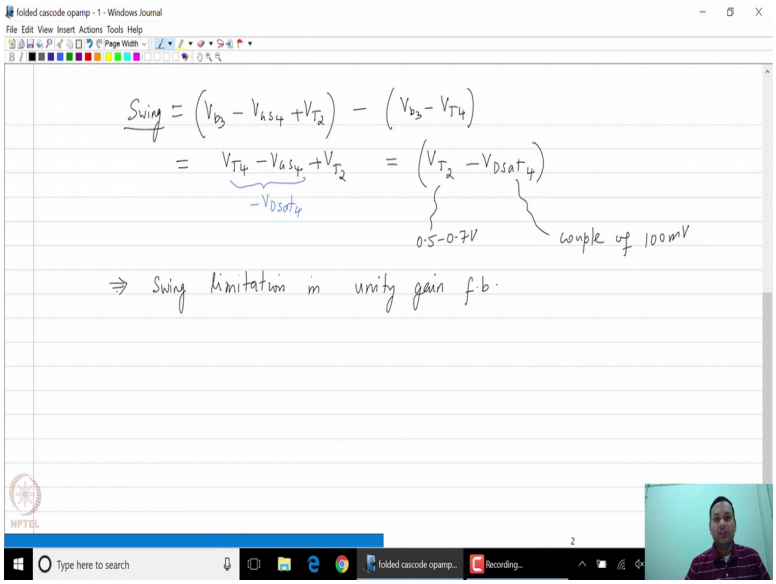

So, the output swing is nothing, but V x plus V T 2. So, V x is V b 3 minus V G S 4 and the minimum value is V b 3 minus V T 4 and this is nothing but V T 4 minus V G S 4 plus V T 2. And please note that this particular expression is nothing, but minus V d sat 4 and therefore, this is nothing, but V T 4 sorry V T 2 minus V D sat 4.

So, this is the maximum swing allowable at the output as you know I know for typical values of transistors this may be a few 100 millivolts let us say 0.5 to 0.7 volts and we know that this is out of the order of a couple of 100 millivolts. So, you can see that this filament is completely independent of the supply and this is only of the order of maybe half a volt or so, irrespective of how large a supply you can get. So, there is a strong swing limitation in unity gain feedback. So, this is a classic problem with telescopic opamps. Now, we want to figure out how to fix this hence you need a different type of opamp.

So, now we will redirect our attention towards the other kinds of cascode structures we have seen before.

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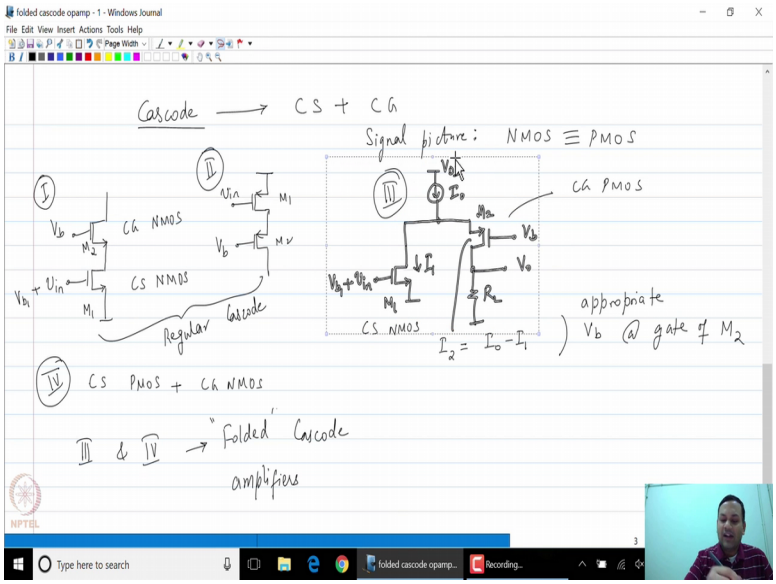

So, remember the cascode structure can primarily be broken down into a common source plus a common gate structure, so that is exactly what a cascode structure is. So, you have 2 transistors the input is applied to the gate of the common source structure and you cascade a common gate structure along with this to give you better output impedance and so on. There are very attractive qualities for the common gate structure. So, I will call these transistors M 1 and M 2 and in this case I have shown a common source NMOS and a common gate NMOS as well.

So, both these transistors are NMOS. But please note that as far as the signal picture is concerned the NMOS and PMOS are identical they have the exact same small signal equivalent circuit. Therefore, you should be able to realize common source common gate combination where each of these transistors could be you know of either type and therefore, we come up with 4 different types of cascode structure. So, this is the first one which is the NMOS cascade. Of course, if you were to draw the PMOS cascode which we have also which we have also seen before. This is the PMOS common source followed by the PMOS common gate and you have 2 more structures the first one we will look at is the case of NMOS of an NMOS common source structure followed by a PMOS common gate structure.

So, the way we can draw it is by since we are used to drawing the PMOS with the source side up with V DD on top and ground on bottom I will draw it in this manner maybe

there is a load resistance R L which I show like this. Now, you also need a bias current source for these 2 transistors and that will be shown as a current source from V DD. Let us say this is some I naught and of course, the gate of the PMOS transistor M 2 is connected to some bias voltage V b.

Now, what are the bias conditions of M 1 and M 2? So, as you can see if M 1 needs a bias voltage that its gate which may be I will represent as V b 1 and this will cause some current I 1 to be the bias condition for M 1. So, therefore, the current through M 2 which is I 2 is given by I naught minus I 1. As you can see the NMOS is biased as the difference between the correct source I naught and the bias current of M 1 and needless to say you should apply and appropriately be and of course, V b 1 at the gate of the PMOS transistor M 2.

And the fourth structure is the PMOS common source followed by the NMOS common gate structure. So, this is the common source NMOS common gate PMOS and you can also build a cascode structure with a common source PMOS transistor plus the common gate NMOS. This is the 4th version. I believe it as a homework exercise it is a pretty straightforward extension of this particular structure.

Now, what is the big difference between the folded-cascode structures? So, these structures maybe I will call them 1 2 3 and 4. The point to note is that 3 and 4 are the socalled folded-cascode amplifiers. Why are they called folded-cascode? Because the way we draw the circuit is such that the circuit is folded down the current is folded down into the common gate PMOS structure from the NMOS. So, that is why these are called folded-cascode amplifiers.

Now, what is the advantage of a folded-cascode amplifier? So, as you can see in the case of the; in the case of the regular cascode structures which are structures 1 and 2 in the case of these regular cascode structures the bias point of M 1 at the input which may be V b 1 and V b are intimately tied together because V b decides when M 1 goes into triode therefore, the input and other bias voltages in the amplifier are somehow related where as such is not the case in the folded-cascode amplifier. So, maybe let us quickly take the structure and let us try to come up with some expression on the bias conditions for this particular amplifier.

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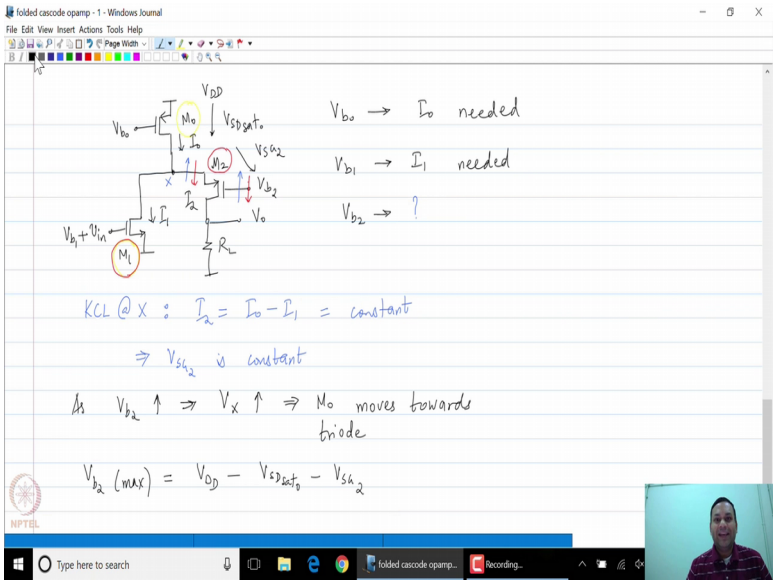

So, let us take this folded-cascode and now let us now modify this because I know that there are no ideal current sources. So, this current source is a bias current from V b flowing into this node. So, that is clearly generated using a PMOS transistor maybe I will call that M 0 and this current is I 0. And of course, the gate of this current source is going to be tied to some voltage V b 0.

Now, of course, the bias conditions V b 0 should be is decided by what current you desire. So, that is decided by I naught and of course, the size of M naught. What about V b 1? It is decided by the value of I 1 that and of course, the width of M 1 that also decides parameter such as g m and so on. What about the current through what about I 2 and n 2? How do you decide V b 2? So, it turns out that there are certain range of V b 2s that can be supported by this particular amplifier. So, let us see what will happen if I start changing V b 2.

Let us say I start increasing V b 2. So, in this structure as you can see if you apply KCL at node x. So, if you apply KCL at node x you can show that I 2 is always that the flux between I naught and I 1 and as long as all transistors are in saturation this current will not change appreciably which means I 2 is constant. Therefore, if I 2 a constant what this means is that the gate source or the source gate voltage of M 2 stays constant which means the voltage at node x starts increasing.

So, as V b 2 increases V x increases and at the same rate and please note that transistor M 1, so transistor M 1 here is moving further and further away from triode. So, you are in no danger of moving that it has a constant current. So, there is no problem with the bias point of M 1, but please note that transistor M 0 is moving closer and closer to triode because its gate voltage is constant and the drain voltage is increasing. So, M 0 moves closer to triode region. So, M 0 clearly moves towards the triode region and eventually it will go into triode. So, the maximum value V b 2 max is clearly given by V S D sat of 0 plus I am sorry, it is given by V DD minus V S D sat of 0 minus V S G 2. So, in other words this voltage is at V DD. So, at the edge this drop will be V S D sat, V S D sat 0 and this voltage is V S G 2 and this will be the maximum value of V b 2.

What is the minimum value of V b 2? So, let us say now that V b 2 starts decreasing, as you can see V x starts dropping and eventually one of 2 things will happen if V x starts dropping as V b 2 drops eventually M 1 could go into triode or the other thing that could happen is that M 2 itself could go to triode as you can see the drain of M 2 is being held constant, but the gate keeps dropping. So, one of these 2 will happen and that will purely depend on the exact bias condition.

So, now that we have a basic understanding of how this folded-cascode works. Let us quickly go ahead and build the opamp out of this folded-cascode. Clearly we built the telescopic opamp using the regular cascade, it should be possible to build an opamp out of the folded cacode also and that is exactly what we are going to look at next.