Analog Integrated Circuits
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Lecture - 31
Telescopic OpAmp – 4

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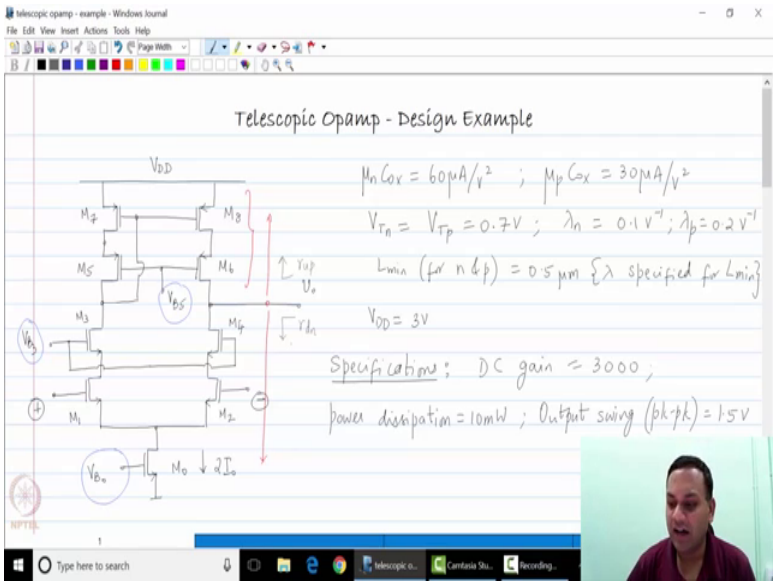

In this lecture we will look at a design example of a telescopic opamp. So, we will assume that the MOSFET process parameters are given to us. So, let us first list them down. So, the MOSFET parameters that are given mu n Cox is 60 micro amp per volt square and mu p Cox is 30 micro amp per volt square and V T n is equal to V T p is 0.7 volts. And we will assume that lambda n is 0.1 volt inverse, lambda p is 0.2 volt inverse and we will assume that L min the minimum length for n and p type transistors is 0.5 microns and lambda is specified for L min and finally, we assume that the power supply is 3 volts.

Now, these are the device parameters. Now, we come to the specifications of the opamp. So, the opamp specifications are as follows. So, we will say that we want a DC gain to be at least 3000, we will say that the total power dissipation is 10 milliwatts and we will say that the outputs swing peak to peak swing is required 1.5 volts. So, these are the specifications that we will start off with.

This will be more of a basic design rather than having the frequency parameters frequency response of the opamp we will first do the basic design of the opamp. Now, the first question would be where we should start. So, of course, always a good place to start is to set the bias current through the transistors. So, we will say that the current, so we will say we will start off at the power budget and we will say that opamp core uses 3 milliamps and the other 330 micro amps will be used for biasing.

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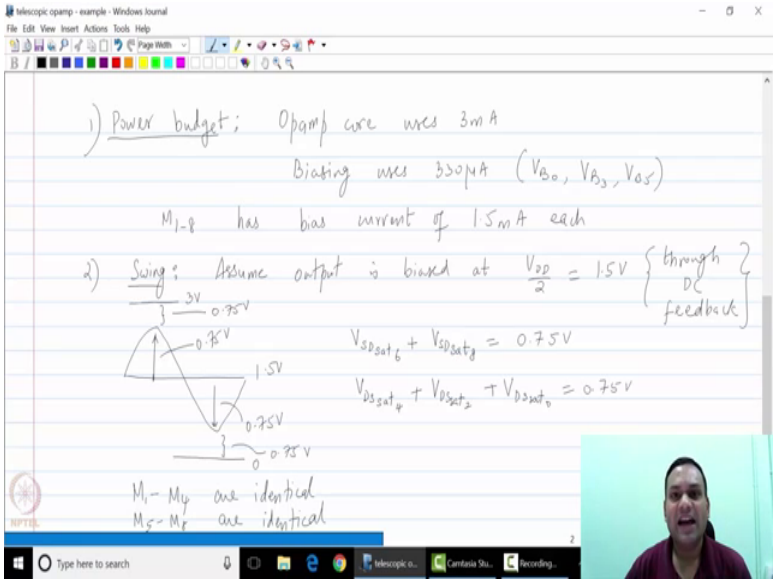

What I mean is that 3 and thirty micro amps is going to be used to generate V B 0 and V B 5 and V B 3. So, of course, you will need to use some kind of reference current source and maybe a bunch of current mirrors to generate these kinds of voltages.

I will not go into the detail, details of how to generate these because these have been seen before, these have been seen before when we had looked at a single transistor circuits and current source. So, let us assume that this is known. So, we will assume that and we will not do that part now.

Now, let us look at the opamp core. So, if the opamp core uses 3 milliamps. So, M 1 to M 8 has bias current of 1.5 milli amperes region. So, that is the first thing to realize this, this current would be equally used as half of half of each side of the opamp. So, this is a good way to start because now we have fixed the bias current. We now need to fix the width and the length of the transistor based and the specifications.

So, the next step what we will do is to look at the output swing. So, the output swing is going to tell us what the V B stack of each transistor is going to be. So, let us assume if every the cache codes are biased such that you have maximum swing possible in the circuits. So, in which case the output voltage can swing up by a certain amount and swing down by a certain amount we will also make some common sense assumptions.

So, we will assume that the output when the opamp is based in it placed in feedback the output is biased at V DD over 2 which is 1.5 volts through DC feedback this is a fairly common sense assumption because you are making sure that the opamp can swing up and down around this V DD by 2 value. Once you do that since we want a swing of 0.75 volts above 1.5 and 0.75 volts below 1.5 as you can see you have M 8 and M 6 above you know going to V DD and M 4, M 2 and M 0 going to ground. So, you can see that if the output were biased at 1.5 volts and it needs to swing to 0.75 volts, so that the on either side. So, that the overall peak to peak swing is 1.5 volts then you will find that the supply between supply and ground you have an additional 0.75 volts at the top and bottom to make up the full 3 volt header.

So, now we need to allocate this 0.75 volts on either side to the appropriate transistors. So, let us now start. So, we can see that when you go look at the upper side you need to ensure that M 8 and M 6 have enough headroom therefore, you can say that, the overdrive voltages. So, let us say at the V D sat, V S D sat of M 6 plus V S D sat of M 8 has to be equal to 0.75 volt. Similarly on the lower end we can say that a V S D sat of 4 plus 2 plus 0 should be equal to 4 plus 2 plus 0 should be equal to 0.75 volts.

Now you need to make a design decision. So, let us first to make our design easier we will assume that M 1 to M 4 are identical this will reduce our search space the design can be refined later based on signal considerations. We will say M 1 to M 4 are identical and M 5 to M 8 are identical again. So, that gives us just a pair of g ms and g dss to design to design for. So, in which case once we make this clear since they have the same widths and lengths and the same bias current they will have the same V D sats as well as the same g ms and g dss.

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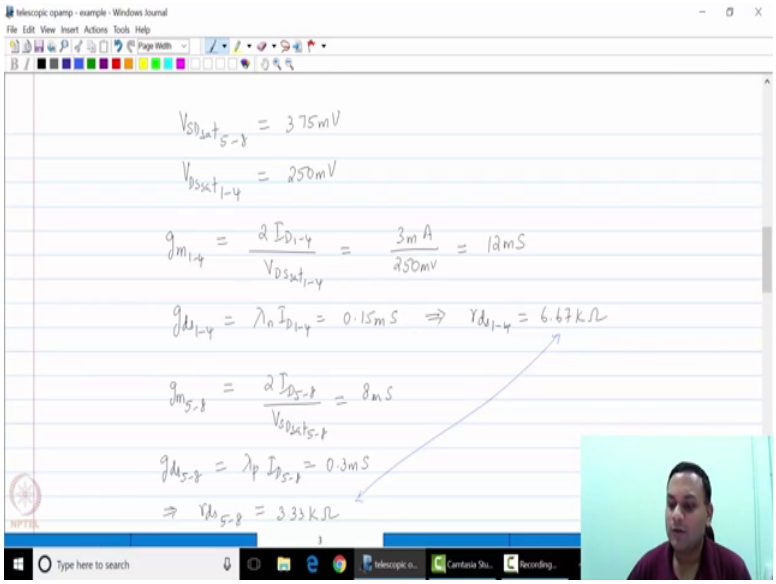

So, the next step is to point out so that V is the sat of 5 to 8 it should now be 375 millivolts and V D S sat of 1 to 4 should be equal to 250 millivolts.

Now, let us start with the signal portion of the circuit and let us say that we want to calculate the g m of the input pair. So, we will write down the g m expression for the input pair as follows. So, this is nothing, but 2 I D 1 over V D S sat of 1 to 4 and this is 3 milliamps over 250 millivolts. Therefore the gms of the input devices is 12 milliseconds.

Now, what do we do next? We can also write down the expression for the g ds of 1 to 4 gds of 1 to 4 is nothing, but lambda n times I D of 1 to 4. So, this is nothing, but 0.15 millisiemens and this means that r ds 1 to 4 is equal to 6.67 kilo amps. So, now, we are in a position to figure out what the requirement of the output resistances.

So, let us do the same thing for the upper transistors also so that we get an idea of the PMOS resistances also. So, if you look at the PMOS resistances. So, we will do the same thing g m 5 to 8 is equal to 2 I D 5 to 8 over V S D 5 to 8. So, this tells us that the g m of 5 to 8 is 8 millisiemens. Similarly g ds of 5 of 8 is lambda p times IDs 5 to 8 and this is 0.3 millisiemens which means that r ds 5 to 8 is of the PMOS transistors is 3.33 kilo ohms. As you can see the PMOS transistors have a lower g m as well as a lower r ds.

So, now, now that we have the cascode transistors we shall also figure out the intrinsic gains of the devices so that we can look at the output resistance of the overall opamp.

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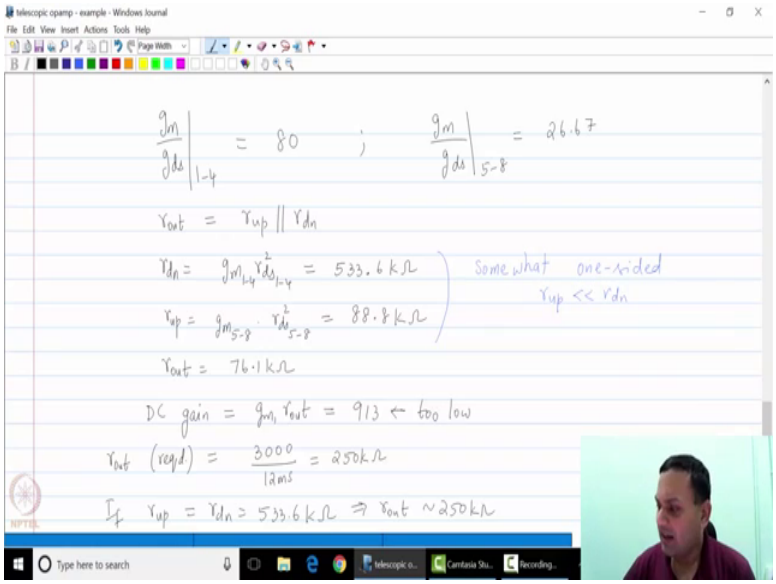

So, g m by gds of transistors 1 to 4 is equal to is equal to 80 and g m by g ds of 5 to 8 is equal to 26.67. As you can see the intrinsic gain of the PMOS transistors is much smaller. This is because we have apportioned higher v gs minus V T for the PMOS transistors which means they should have a smaller size and for the same current they will have a smaller g m and because the lambda of the PMOS is larger than the lambda of the NMOS it turns out that the gds is a larger for the same bias current and the r ds as small. Therefore, what you are seeing is for this particular setup for these particular set of the device parameters and the particular design we are looking at the intrinsic gain of the NMOS transistor is much larger than that of the PMOS transistor.

Now, based on this we will now say that the impedance looking upwards which is I will denote by r up and the impedance looking down I will denote by r down. So, we can write the overall output resistance r out is r up parallel r down. And what is r down? r down is g m into g m 1 to 4 into r ds square 1 to 4 and this particular value ends up being equal to 533.6 kilo ohms. Similarly, r up is g m 5 to 8 times r ds square 5 to 8 and this number ends up being 88.8 kilo volts.

Now, there are a few things we should note the first thing we should note is that the up and down resistance are fairly one sided. So, that is something we should note. So, the up resistance is much much smaller than the down resistance. So, this means that the actual effective DC gain of the op amp is more or less going to be limited by r up and in many

designs you do not want it to be skewed in this manner. Because then the impedance looking down you know does not contribute to the, in other words the intrinsic gain on one side is much larger than the other and therefore, the effective gain you can extract out of the circuit is much smaller than what you expected. So, if you were to look at our route is r out parallel r down and that value ends up being 76.1 kilo ohms.

Now, we are now at the position to calculate the DC gain. The DC gain magnitude is g m 1 times r out and this number is ends up being approximately 930 this is clearly too low for our design we are expecting a gain of around 3000. So, now, what do we do? So, we can do several things the first thing we will look at is what does that DC gain what is the r out that is required to reach a DC gain of 3000.

So, let us look at that let us look at the inverse problem. So, the r out required is equal to DC is equal to 3000 over 3000 over 12 millisiemens this is approximately 250 kilo ohms. Now, the reason we are going this path is because the difference between and the required DC gain and the DC gain we are we have achieved is so large that it seems like our original design our original expectation is quite different from what we are getting right what we need.

So, therefore, we are going to try a different approach. So, now, let us try this you know let us compile this required r out 250 kilo ohms with the numbers we have seen. As you can see if, so if r up was equal to r down, in other words if r up equals r down equals 533.6 kilo ohms, if both of these were 533.6 kilo ohms you can see that around r out is approximately 250 kilo ohms. In fact, it is slightly larger than 250 kilo ohms, so in fact, now our job is clear we should actually be trying to increase r up such that it is almost equal to r down. So, let us look at how we can do that.

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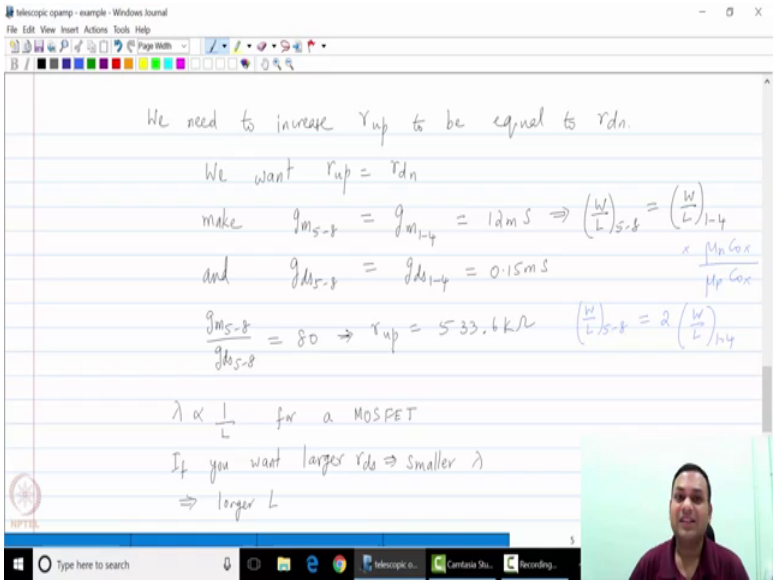

So, we need to, we need to increase r up, r down. So, now, we will take the opposite approach. So, we will say let us make it exactly equal to r down. What does that mean for us?

So, we want r up equals r down the easiest way of achieving this is to make g m of transistors 5 to 8 equal to g m of transistors 1 to 4 and make gds of 5 to 8 equal to g ds of transistors 1 to 4 if you achieve this you can rest assure that r up will also be equal to 533.6 genomes. So, let us now ensure that this happens. So, if we were to do this then what we are saying is that we want r up g ms of the PMOS transistors to also be equal to 12 millisiemens and we want the g dss to also be equal to also be equal to 0.3 millisiemens, sorry we want the gds to also be 0.15 millisiemens. If we ensure this then g m 5 to 8 by g ds 5 to 8 will also be equal to 80 and this means r up will become equal to 533 kilo amps. So, this is again a design constraint that we are going to apply.

Now, our final job is to figure out whether this will actually meet our design requirements. So, first of all the first step is to see how you make g m 5 to 8 equal to g m 1 to 4. So, this means since they have the same bias current the W over L ratio of 5 to 8 should be equal to the W over L ratio of 1 to 4. So, this is easy to achieve you choose the width such that the, width to length ratio such that they are equal.

Now, what about the second condition this is a little bit harder to achieve because fundamentally the 2 devices have a different lambda. So, the first step is to try to achieve

a larger or put resistance. So, what we know we will point out we know from basic device physics that lambda is proportional to the inverse of the length of the device. So, now, what this means is that we want if you want larger r ds. So, this means smaller lambda and this means longer L. So, now our job is clear we need to increase the length of the PMOS transistors such that they have a smaller lambda and you get a larger r ds. How much do we need to increase the length, now that is given by the ratio of lambda p over lambda n. So, lambda p was 0.2 volt inverse for L equals 0.5 microns.

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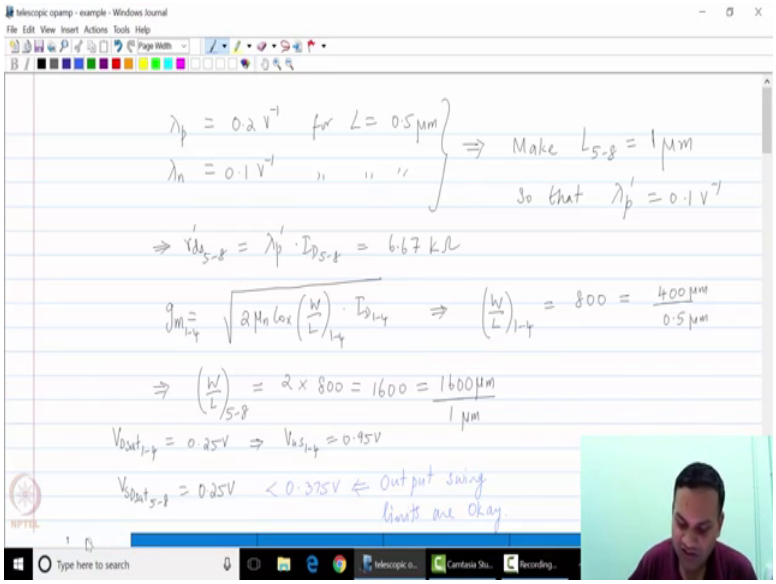

So, now, since we wanted to double the resistance, let us look at r ds of 5 to 8 and 3 to 4 you can see that there is a factor of 2 separating these 2. So, we want lambda of the PMOS to so be equal to lambda of the NMOS. So, that you get the same r ds to do that since and we know that since we know that lambda n has 0.1 volt inverse for this. So, this tells us make the length of the PMOS transistors should to be equal to 1 micron so that the new lambda I will call that lambda prime is 0.1 volt minus L.

And once you do this once you set the length of 5 to 8 transistors, 5 to 8 which are the PMOS transistors to be equal to one micron the lambdas will now be 0.1 volt inverse and we can calculate the new r ds prime for 5 to 8 will be equal to lambda p prime times I D 5 to 8 and this will also be equal to the 6.67 kilo ohms.

Now, the next step is to set the g ms to be well we have now said that g m of 5 4 6 to 8. A small correction here this is true, there is a small correction here please note that this is

not correct this should be in the ratio of the mu n Cox. I will make that correction separately into the ratio of mu n Cox over mu p Cox. Please note this correction I have erroneously said that the width or length ratio of 5 to 8 will be equal to width or length of 1 to 4. They should actually be in the ratio of the mu n Cox.

In that case, this tells us that. So, W over L of 5 to 8 should be 2 times W over L of 1 to 4 this is the width to length ratio now we can calculate the value of width to length ratio from 1 to 4 from the value of the g m of the device. So, let us do that. So, we will start from the basic g m equation to mu n Cox W over L times I D 1 to 4 and this tells us that the width to length ratio for transistors 1 to 4 should be equal to 800. So, this tells us that they should be 400 micron over 0.5 micron. This is because we had chosen the length of the transistors to be 0.5 microns. This means that W over L of transistors 5 to 8 should be 2 times 400 by micron 2 times 800, which is 1600. So, this is nothing, but 1600 micron over 1 micron because we had chosen the lengths of these devices to be 1 micron.

Finally, we have to go back and calculate the V D sats of the devices because now we have changed the sizes of the devices. So, if you go back and calculate the V D sats of the devices, so V D sat of devices 1 to 4 is equal to 0.25 volts as we have said this and this gives us V G S 1 to 4 of 0.95 volts. Now, this V G S and we decide number these numbers will be used to set the values of V B 3 and V B 5 and V 0.

Now, what about V S D sat of 5 to 8, it turns out that since everything both g m and current values have been said to be equal. So, this is also 0.25 volts and it turns out that this is less than the required value for the swing which was 0.375 volts. So, therefore, output swing limits are ok. So, now, this particular design will meet all specifications required from the original opamp. So, the final requirement is to set the values of V B 3 and V B 5, I will leave that as a homework exercise.

I just want to point out we have still not decided the size of M 0. So, one easy way to set the value of M 0 is to say that M 0 has 0.25 volts V D sat and twice the current as M 1 to 4. So, it is meant to have the same V D sat due to the swing limits that we have imposed and it carries twice the bias current.

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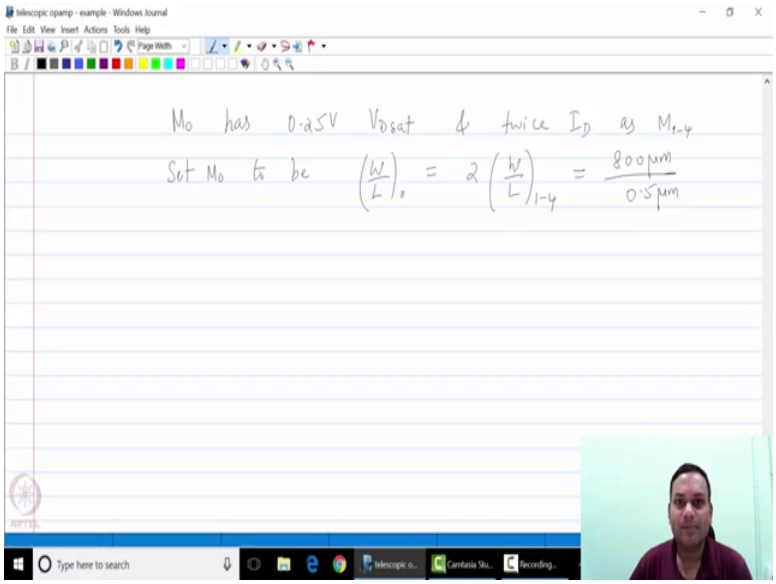

Therefore you can say that M 0, so you can set the width to length ratio of M 0 to be twice width to length ratio n of transistors 1 to 4 and this is nothing, but a 800 microns over 0.5 microns. So, this completes our (Refer Time: 31:04).