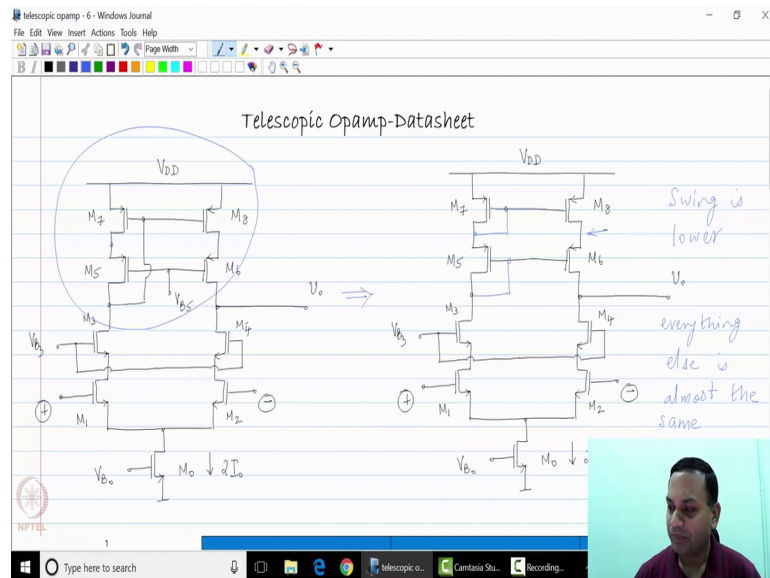


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Lecture – 30
Telescopic OpAmp – 6

(Refer Slide Time: 00:17)



In this lecture, we are going to build the data sheet of the a telescopic Opamp that will be discussing so far. Before we do that let us look at 1 or 2 more aspects of the telescopic Opamp before the go forward. The first point that we are going to learn is it is possible, so far we have been building the we have been using the high swing version of the current method, it is of course, possible to build the low swing current mirror the biasing is just a little bit simpler, the low string version would be as follows. So, you are going to take this portion and create the low swing or the easier version of this. So, that will look as follows.

So, we will take this Opamp and instead of creating this feedback to create the high swing node, we will simply use 2 diode connected devices on the left hand side as the (Refer Time: 01:22) in this. So, this will not require a separate V B 5 we have seen what the value of V B 5 should be in the current mirrors lecture. So, as you can see this requires 1 less bias voltage, but the voltage at this node will be higher than the original case and therefore, this swing is lower compared to the original version compared to be

left hand side figure. So, that is something to keep in mind it is just a little bit easier everything else is the same everything else is almost the same. There will be some small differences, but more or less they are the same circuit except for this particular biasing reference.

(Refer Slide Time: 02:22)

Next I will also find point out that it is possible to build what is called a triple cascode amplifier. So, similar to the telescopic amplifier with a single cascode device, it is all it is also possible to add double cascode or a triple cascode device. So, you can add 1 more set of cascode devices on top of the original amplifier cascode to create this amplifier. So, this would have again as you might imagine the game would be of the order of gm rds the whole cube.

So, this would be give you even larger DC gain; however, the if you had a load capacitance C L, the it would turn out that the overall transconductance does not change and the unity gain frequency omega u is still gm 1 over C L that does not change, and this only gives you know better DC gain compared to the original circuit. Of course, now that you have added a extra set of 2 devices in series from VDD to ground.

So, this circuit is expected to have much lower springs of course, r out is much larger, but from this you would also expect at low frequencies you expect no addition and noise from the unix cascade extra cascode devices. Finally, I want to point out because the

circuit has much lower swings it is not very useful for low VDDs. So, VDD less than maybe 2 or 3 volts for VDD less than 2 or 3 volts this circuit is not very useful.

So, you do not see it very often finally, even an older generation processes where you did have the supply headroom to use. So, that circuit there are some limitations you cannot just keep adding cascode devices, because at the end of the day there are parasitic diodes reverse bias diode hanging off the drain and sources of every transistor, and that it would turn out that the impedance of those devices would limit the overall impedance at the output node.

So, I will show them here. So, these are the parasitic diode reverse bias diodes of m_5 and m_6 . So, they will have some r_t they will have some dynamic resistance, which will come in parallel with the cascode resistance. As you keep adding more cascodes the value of r_d does not change because each device has its own fixed parasitic reverse bias diode therefore, there is not much value to add larger and larger stack of devices.

(Refer Slide Time: 06:14)

PMOS Telescopic Opamp

- * need larger PMOS transistors for same g_m
- expect non-dominant poles & zeros to be smaller compared to NMOS case
- For same W/L , expect PM to be smaller
- * Input CM range of PMOS version is different

The circuit diagram shows a PMOS telescopic opamp. The input stage consists of PMOS transistors M_1 and M_2 in a differential configuration. The cascode stage consists of PMOS transistors M_3 and M_4 . The output node is connected to a PMOS load transistor M_0 and a PMOS cascode transistor M_5 and M_6 . The circuit is biased with V_{DD} , V_{BS} , and a current source I .

Next I wanted to point out that it is possible to build the P MOS telescopic Opamp similar to the possibility of building and single stage Opamp with P MOS input stages it is also possible to build a telescopic Opamp with a P MOS input stage because the signal characteristics of the Opamp is of the n mos transistor and P MOS transistors are the same therefore, if you build a telescope Opamp with P MOS transistors you expect these signal characteristics to be the same, you expect that DC characteristics to be the defect.

So, we will draw the P MOS amplifier here. So, and the input goes to the P MOS transistors shown here, I will call them m_1 and m_2 and let us say this is the positive and this is the negative terminal of the Opamp, and the Opamp is biased with a current source of value $2 I_{naught}$, and as you can see this is the cascode cascode amplifier and we call them m_3 and m_4 and m_5 , m_6 , m_7 and m_8 are the n mos current mirrors.

So, let us appropriately add the feedback. So, m_5 and m_7 will have a bias voltage V_{B5} applied to the gates, they are the cascode transistors and the gates of m_1 of m_7 and m_8 are biased using feedback. So, to create a high swing current mirror the output is of course, taken from the drain of m_6 and m_4 apart from this the signal characteristics of the same there is one point to remember. So, you need larger P MOS transistors for the same g_m therefore, you need you expect that the non dominant poles and zeros to be closer compared to the earlier case. To be smaller I mean closer into the origin and therefore, for the same phase margin in unity gain you expect the ω_u to be to be smaller or rather I maybe I should put it in a different way because we are comparing for the same g_m , for the same ω_u you expect that the phase margin to be smaller.

So, in other words you will need to pull in the ω_u you need to reduce ω_u to achieve the same phase margin. So, that is another point and finally, of course, the most important point of this is that the input common mode range of the P MOS version is different, because the you expect the input of the P MOS device at a different bias voltage compared to the n mos device and that can easily be calculated for this particular circuit.

(Refer Slide Time: 11:48)

Data sheet

- 1) DC gain = $g_{m1} \cdot r_{out}$
 $r_{out} = (g_{m6} r_{ds6} \cdot r_{ds8}) \parallel (g_{m4} r_{ds4} \cdot r_{ds2})$
- 2) UAF $\omega_u = \frac{g_{m1}}{C_L}$
 $\omega_d = \frac{1}{r_{out} C_L}$
- 3) Non-dominant poles & zeroes - several additional poles & zeroes.

first ND pole is at $X = \frac{g_{m7}}{C_X}$

So, now we will take a high swing current mirror the telescopic Opamp with the high swing current mirror and build the datasheet for that particular Opamp. Now let us assume that the currents and sizes are known. So, now, we are in a position to build the datasheet. So, the first characteristics that we are interested in is the DC gain even though I say in DC gain, I want to reemphasize that this is actually the low frequency gain I am not the gain if you apply a DC voltage at the input.

So, of course, you can apply an incremental DC voltage at the input and achieve the same DC gain. So, the DC gain of the Opamp is g_{m1} times r_{out} where r_{out} is nothing, but $g_{m6} r_{ds6}$ times r_{ds8} , in parallel with $g_{m4} r_{ds4}$ times r_{ds2} . So, it has a very large output resistance, but to the unity gain frequency ω_u is g_{m1} / C_L , where C_L is the load capacitance that is being driven and c . Of course, the dominant pole ω_d will be $1 / (r_{out} \times C_L)$, and as you can see the dominant pole and the ω_u are related to the DC gain of the amplifier by writing this we are assuming that the non dominant poles occur at a much larger frequency compared to ω_u .

What about non dominant poles and zeroes, as we have seen you expect this system to have about a total of 6 poles. So, and several zeroes because you have multiple paths. So, there are several of them several additional poles and zeroes and we point out that the first non dominant pole is that node x which is basically. So, this the position of the pole is g_{m7} / C_x that C_x is the total capacitance at node x overall.

(Refer Slide Time: 14:53)

4) Input-referred noise voltage: $e_n^2 = \frac{16kT}{3g_{m1}} \left[1 + \frac{g_{m7}}{g_{m1}} \right]$

* to reduce noise e_n
 \rightarrow increase g_{m1} (affects signal)
 \rightarrow decrease g_{m7} ; I_0 remains the same

5) Input-referred offset voltage $v_{osn}^2 = v_{i,2}^2 + \left(\frac{g_{m7}}{g_{m1}} \right)^2 v_{i,7,8}^2$

* to reduce offset voltage
 \rightarrow decrease $\left(\frac{g_{m7}}{g_{m1}} \right)$

$V_{DSat_{7,8}}$ increases $\left(\frac{V_{i,7,8}}{I_{7,8}} \right)$
 available output swing limits reduce

The fourth parameter that will right is the input referred noise of the telescopic Opamp; as we have seen the input referred noise e_n squared has 2 components you have the component from m 1 and m 2 you have the component from m 7, and m 8 and as we saw the component from m 3, m 4, 5 and m 6 do not appear as an input referred noise at low frequencies. Because we gain or rather the path the current noise takes to the output is such that they get cancelled at the output short circuit node.

So, the overall the input referred noise voltage in squared is $16 k T$ by $3 g m 1$ times 1 plus $g m 7$ over $g m 1$, and as you can see now we also know what to do to reduce noise. So, to reduce noise you will need to increase $g m 1$ as much as possible and you need to decrease $g m 3$ as much as possible. Now please note that increasing $g m$ affects the signal whereas, $g m 3$ is the sorry this should be $g m 7$.

Since this is the telescopic Opamp you are trying to decrease the $g m$ of these 2 transistors and increase the $g m$ of m 1 and m 2. Now it should be noted that m 1 and m 2 are part of the signal path and the $g m$ will affect this DC gain as well as the unity gain frequency. However, you notice that the value of $g m$ of m 7 and m 8 do not directly affect the signal characteristics such as DC gain and unity gain frequency and therefore, it is possible to minimize the it is possible to minimize $g m 7$ without affecting the signal too much.

However there is one catch. So, if you decrease g_{m7} , I_{naught} stays that remains the same in such a situation you will find that the $V_{SD sat}$ of 7 and 8 increases, and this means the available headroom in other words available output swing limits are affected. So, in other words you are basically saying that the minimum voltage that m 8 can have before it hits the edge of the triode region is getting larger and larger because as you can see for the same current I_{naught} to decrease g_{m8} or g_{m7} , you need to decrease the size of w over L .

So, I will write that down this manner. So, w over L or 7 and 8 decreases and $V_{SD sat}$ increases; and this means the minute $V_{SD sat}$ increases the available output swing limits will definitely reduce. So, that is something to keep in mind that is a point beyond which you cannot reduce g_{m7} further. So, next we will look at the input referred offset. So, as we saw again this had 2 components the input referred offset squared which is the standard deviation of the input offset had 2 components.

The component from the input devices 1 comma 2 appears directly at the input, and the component from 7 and 8 appears at the put with scaling factor g_{m7} over g_{m1} the whole square. So, again if you want to reduce the input referred offset voltage you need to reduce the V_T offset v_d mismatch between the input transistors you also need to reduce g_{m7} over g_{m1} .

So, you need to decrease g_{m7} over g_{m1} . As you can see decreasing this factor g_{m7} over g_{m1} would reduce both the input referred offset voltage and the input referred noise voltage.

(Refer Slide Time: 20:50)

6) Slew rate :
positive & negative $SR = \frac{2I_{D0}}{C_L}$

7) Input CM range : $\left\{ V_{Dsat0} + V_{GS1}, V_{B3} - V_{GS3} + V_{T1} \right\}$

8) Output CM range : $\left\{ , V_{B5} + V_{T6} \right\}$

The next data sheet parameter we will look at is the slew rate of the Opamp, as we have seen the positive and negative slew rate are both equal for this Opamp and it is equal to $2 I_{D0} / C_L$. The input common mode range is the next quantity, we have seen that the minimum input common mode is achieved when m_0 just hits the edge of triode region, and at that point the minimum input common mode range is $V_{GS1} + V_{Bsat0}$.

So, this is the minimum input common mode range and if you were to start increasing the input common mode. So, if you were to start increasing the input common mode eventually m_1 and m_2 will go into the triode region and the edge of that region comes at a time when the gate of m_1 goes larger than its drain by $V_{GS1} - V_{D1}$. So, the gate of the transistor is a dc in. So, that happens at $V_{B3} - V_{GS3}$ this is the drain of m_1 plus V_{T1} .

So, this is the input common mode range similarly the output common mode ranges as follows. The output common mode range the maximum output common mode range in this particular situation is when m_6 hits the edge of triode region, that is simply $V_{B5} + V_{T6}$. Simply $V_{B5} + V_{T6}$ or V_{T6} and the minimum output common mode range happens when m_4 hits the edge of triode region that happens at a voltage of $V_{B3} - V_{GS4}$.