Analog Integrated Circuits
Prof. S. Aniruddhan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 03
MOSFET Current Mirrors

In the previous lecture we stopped with a small brief discussion of current mirror circuits. So, in this lecture we are going to take that forward to see a few different types of current mirrors. So, first we will start off by drawing the basic current mirror that we looked at in the previous class.

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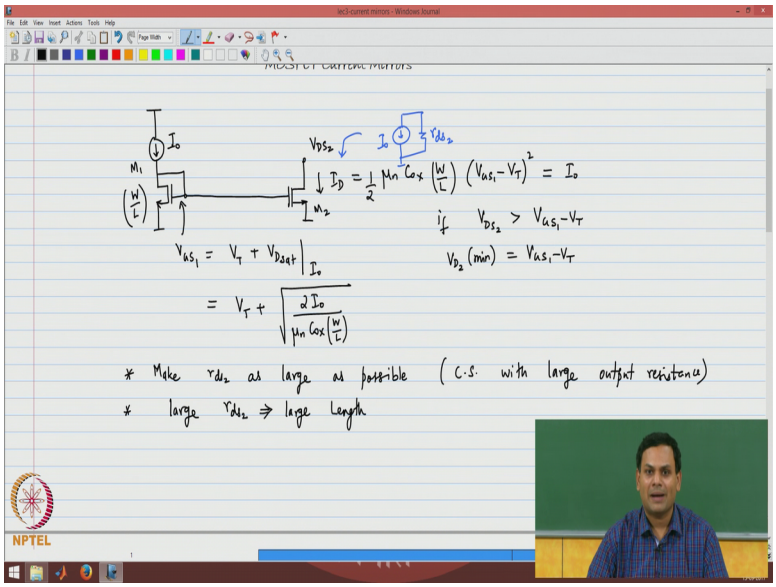

So, if you take a current I naught and pass a through a transistor with a certain width over length, this will generate through a feedback action this will generate a voltage V GS I will call it V GS 1 and I will call this transistor M 1.

This will generate a voltage V GS 1 that will correspond to a drain current of I naught. So, this will clearly be V T plus V D sat at a current I naught, this is nothing but V T plus this will be the voltage generated. Now, this voltage can now be applied to a second transistor which will now have a current a drain current that is related to the gate source voltage as half mu n C ox W over L into V GS 1 minus V T the whole square.

Now, if you ignore the dependence of the drain current on the drain source voltage this will clearly be equal to I naught. Now, this assumes that the drain source voltage for the second transistor is large enough such that it is not saturation. So, this assumption is made. The transistor M 1, transistor M 1 is always in saturation because the drain voltages equal to the gate source voltage. So, this was a simple current mirror we saw last time.

Now, this current mirror can be used to bias are the circuits for example, this portion of the circuit looking down looks like a current source with a very large resistance, the value of the resistance is the output resistance of the MOSFET which is r ds 2. So, this transistor M 2 to the rest of the circuit presents itself as a current source with some r ds 2. So, if you want the bias circuit look ideal, if you wanted a look like an ideal current source you need to make r ds 2 as large as possible. So, this is going to be one of the design constraints.

Now, normally r ds 2 of course, depends on the bias current, but since we are constrained to have a bias current of I naught r ds 2 large r ds 2 also means large length because as it turns out the longer the transistor is longer is the length L larger will be the r ds 2, but that is a certain limit beyond which you cannot increase r ds 2. Suppose I want to get even better output resistance, so you want to get a current source which has as large an output resistance as possible. So, that is our goal. So, we now want to make r ds 2. Now with a single transistor there is only so much you can do with r ds 2 beyond that you cannot increase r ds 2 any further. So, we want to look at circuit methods to increase r ds 2.

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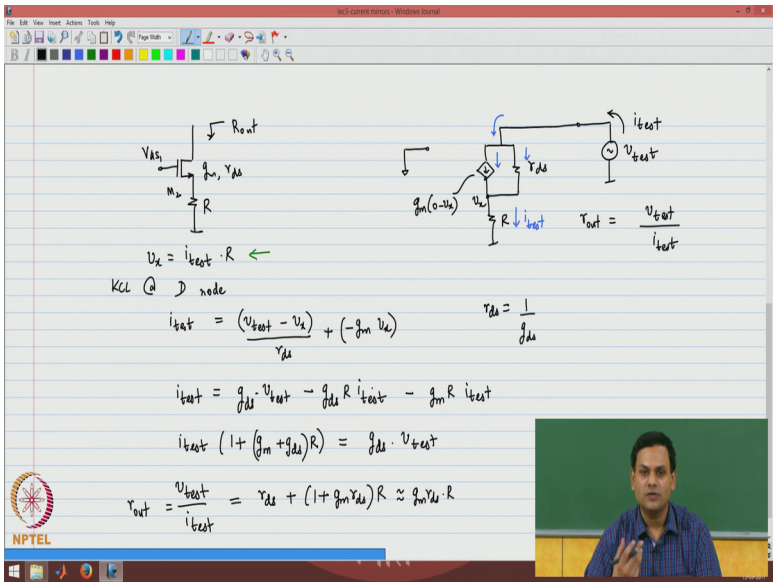

One way to do that is to use a different circuit technique. Now, to do that let us start by adding a resistance R in the source path of the transistor M 2, this was V GS 1 which is the same as V GS 2. I am going to add a resistance R in the source path of M 2 and now want to find out what the output resistance is for this particular configuration.

So, let us assume that the transistor has a gm and an r ds. So, now, to find out the small signal output resistance I will draw the small signal equivalent circuit V GS 1 is generated by the current mirror the mirror portion the left side portion of the current mirror that will be at signal ground. I am going to call this voltage V x. So, that this current source is going to be at gm times 0 minus V x.

I want to find out the output resistance looking in from the drain of the transistor M 1 and the way I do that is I am going to connect a test voltage we test a small signal test voltage and I want to find out what the current drawn by the circuit is so that my small signal output resistance can be calculated which is also the Thevenin resistance can be calculated in this form as v test by i test.

Now, to do that, I am going to note is several things I am going to note that the current i test flowing in is going to split into two paths in this way and eventually is also going to flow through the resistance R. So, it clearly the current flowing through R is also i test. So, I will point out that is equal to i test times R. Then I will perform KCL at the 2 nodes to figure out what the relationship is between v x v test and i test. So, I am going to

perform KCL at the drain node those of you who have seen the voltage controlled current source or a source degenerated circuit will know this expression already, but I am doing this for the benefit of all the others who have not seen the circuit before.

So, the current flowing in is i test that splits as v test minus v x by r ds that is the current flowing in the right side portion of the circuit plus minus gm v x. So, now, I am going to write for ease of writing the equations I am going to say that r ds is 1 over g ds. So, that i test can be written as g ds times v test minus g ds times v x and I am going to write it in this form. v x I am going to replace with this expression and now I am going to group together all the terms of i test on one side I am going to write the slightly simplified version as we go along plus in other words this R out expression is nothing, but small r ds plus capital R plus gm r ds times R and as you can see this is a dominant term is since gm r ds is the intrinsic gain of the transistor this is the dominant term among all of these terms and I will write this as approximately being equal to gm r ds times R.

So, note that if I add a resistance looking in at the drain if I add a resistance at the source the impedance looking in the drain is a magnified form of this resistance. So, now, I can of course, use this because I can now create a current mirror in this form.

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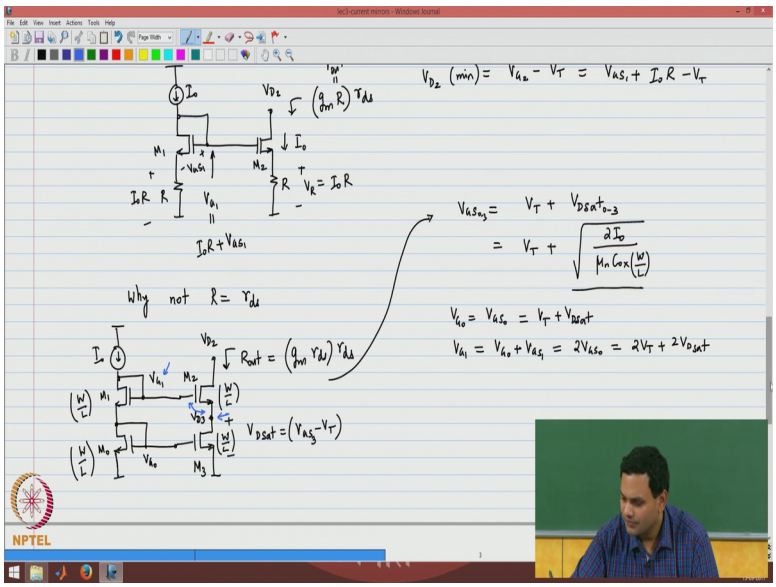

I will need symmetric circuits on both sides, so I will need to add the resistance r on both sides. If I do this I will earlier the resistance was r ds now I have I am going to write it in

terms of the earlier resistance, I will get an output resistance which is equal to gm R times r ds which hopefully will be larger than r ds itself.

So, now I have managed to create a current source, remember that this current is also I naught. I have manage to create a current source which will have a much larger output resistance, but there is one problem. The minute I put a resistance here the voltage drop across the resistance is the DC voltage drop across the resistance is equal to I naught times R. So, if I try to get very large output resistance by increasing the value of R the voltage drop across the resistance also increases and eventually what will happen is that the minimum value of V D 2 will get affected. Because as V R increases V GS 1 or rather I now I am going to call it V G 1 the gate voltage is equal to I naught R plus V GS 1.

Note that I have a voltage I naught R here and I have a voltage V GS 1 here. So, at the gate of M 1 and M 2 I will have a voltage which is I naught R plus V GS 1 and therefore, the drain voltage can only have a minimum value of V G 2 minus V T, i e it is V GS 1 plus minus V T. In other words this is the minimum value of V D 2.

What was the earlier value of minimum value of V D 2? In the earlier circuit the minimum value of V GS 1 was V GS 1 minus V T now you have an extra term I naught R. So, clearly what is happening is it looks like a better current source, but now the voltage compliance at the output has now gotten worse. So, I cannot arbitrarily increase the resistance R I need to find out a different way of doing this. So, now I want to get a large resistance R. So, the next question is instead of using physical resistance R why not use a drain source resistance of a MOSFET itself. In other words I am going to use the small signal resistance drain source resistance of the MOSFET to generate this R hopefully in DC it will look better let us look at this, if I look at this R out of this circuit this is clearly going to be gm r ds times r ds which is going to be very large hopefully much larger than the earlier number.

What about the voltage here? All I have to ensure is that this lower transistor here now let me name them name this M 3 this was M 2, all I have to do is I have to ensure that this transistor has a voltage equal to V D sat which is V GS 3 minus V T. If I ensure that a voltage V D sat is maintained between the drain source of M 3 I am assured that M 3 is in saturation and therefore, it will have a an output resistance of r ds the small signal model will be valid.

So, now I am going to draw the rest of the circuit because we have not shown M 1, this is M 1 now note that I need to generate a voltage for M 3 and I am going to generate that using a fourth transistor, a forth transistor I am going to call it M 0 since it is from the left side. Now, I still need to connect the gates the common gates of M 0 and M 3 to some node and this happens to be a convenient node. So, now, I can calculate what the voltages are in the rest of the circuit. So, let us quickly do that I am going to do the analysis for it here up here.

So, note that V GS naught as I am going to assume for this I am going to assume that all transistors have the same width and length. So, note that V GS for all transistors 0 to 3 is nothing, but V T plus V D sat 0 to 3, this is V T plus root of 2 I naught over mu n C ox W over L. Since all transistors have the same bias current this and the same width and length, this V GS will be valid for all transistors.

So, now, I need to find out what the bias voltages are in the different parts of the circuit. So, clearly the output voltages sum drain voltage its sum V D 2. Now, I will denote this voltage by V D 3 this voltage by V G naught and this voltage by V G 1 and I am liberally going to use the term V D sat because this much easier to use instead of writing the current expression in terms of currents and mu n C ox. So, the first thing I can write is V G naught is equal to V GS 0. So, the gate of M 0 and the gate of M 3 of course, then are biased data voltage V GS naught. So, this is V T plus V D sat.

Now, V G 1 which is the gate of transistor M 1 here is at a voltage of V G naught plus V GS 1 in other words it is biased at V GS naught or 2 V T plus 2 V D sat. What about V D 3? The V D 3 the voltage at the drain of M 3 is going to be biased at 1 V GS 2. So, I am going to find out V G 1 and then subtract V GS 2 from that that will give me V D 3.

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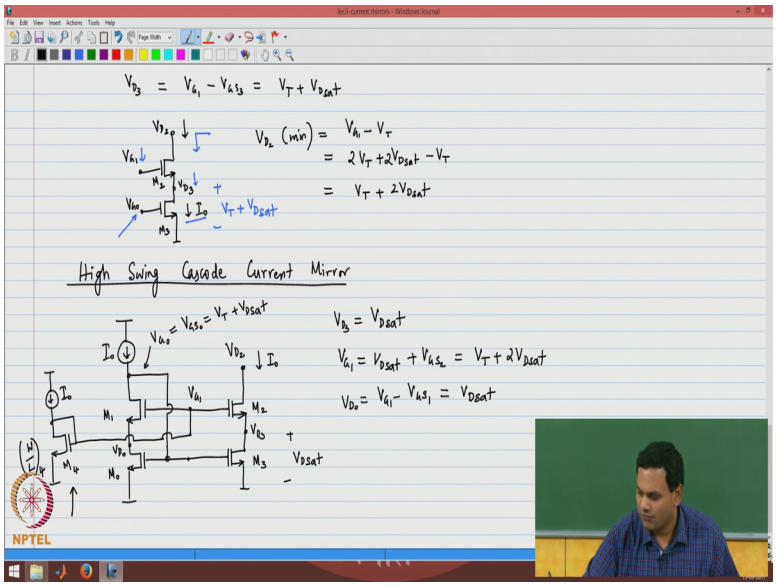

So, note that from KVL V D 3 is equal to V G 1 minus V GS 3 and this is equal to V T plus V D sat again. So, in other words the voltage at the drain of M 3 is at a voltage not V D sat, but V T plus V D sat. So, it is at 1 V GS above ground.

Now, if I start reducing the voltage at the output let us see what happens I am just going to look at the output note. So, I am going to start reducing V D 2 and if I do this note that the voltage at the gate of M 2 which is V G 1 does not change. The voltage of the gate of M 3 does not change and because M 3 and M 2 are carrying a nominal current of I naught the voltage at the drain of M 3 also does not change. So, please note that if I start reducing V D 2 as long as the current does not change by a large amount V G 1 V G naught and V D 3 do not change. So, eventually the minimum value of V D 2 is clearly V G 1 minus V T or 2 V T plus V 2 V D sat minus V T or V T plus 2 V D sat. This is the minimum voltage possible at the drain of M 2 before M 2 goes into the triode region. Once M 2 goes into the triode region you are not assured that the output resistance is still very large. Please note that the output resistance will be large only if all transistors r in saturation.

Now we have seen that V D 2 minimum is V T plus 2 V D sat, but note that M 3 still has a voltage V T plus V D sat across it and actually M 3 can be in saturation even with a voltage of just V D sat across it therefore, I should be able to push down the voltage compliance of this current mirror even further.

I need to do it by changing the bias voltages in the circuit, clearly this voltage V G naught cannot be changed because I require that to support a current I naught in the circuit. However, the only way V D 3 can be reduced is by reducing V G 1 so I need to find out a different way of producing V G 1. Clearly my original method of making this connection these two connections may need to be changed because I cannot afford voltage of 2 V T plus 2 V D sat at the gate of M 2.

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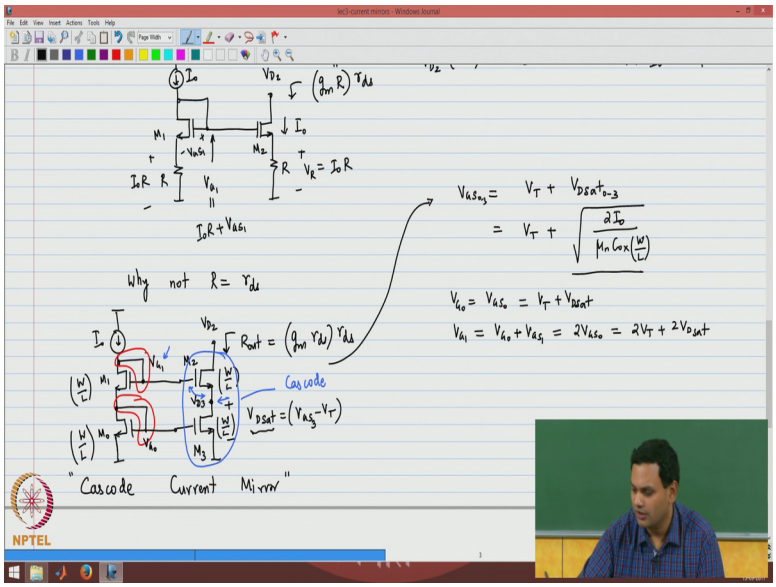

So, we come to the final very oftenly you a very often used circuit which is called the high swing cascode. So, this note that this connection this circuit is called the cascode current mirror, the configuration where you have 1 transistor stacked on top of another in this configuration is called a cascode and this circuit is called a cascode current mirror the next circuit we want to look at is what is called a high swing cascode clearly we still need the stack of two transistors on both sides to generate the large output resistance.

However I want to change the bias voltages at these two nodes. So, the first thing I need to do is I want this to be bias low enough such that the drain source voltage across M 3 is only equal to V D sat. Number 2 I want a current I naught to be drawn from the output. So, I want good mirroring action I want V D 2 to be as low as possible to be able to swing as low as possible, so to do that we are going to use a different feedback connection. So, if you make this connection this will ensure that this voltage V G 0 will

still be equal to V GS 0. So, this is also a case of negative feedback just like the original current mirror this voltage will be equal to V T plus V D sat.

Now, we still have a problem of generating this voltage which is V G 1. So, the way we do it is we will use a third or a or a fifth transistor to generate this voltage, I am going to call this W over L of M 4 W over L 4 for transistor M 4. Now, we know the condition now. So, we wanted V D 3, we wanted V D 3 to be V D sat, so that transistor M 3 is exactly at the edge of saturation we want therefore, we want V G 1 which is this voltage we wanted the gate of M 1 and M 2 to be at a voltage equal to V D sat plus V GS 2 in other words this should be equal to V T plus 2 V D sat. Note that V GS 2 is V T plus V D sat. And if this happens the drain of M 0 which is I will call V D 0 V D 0 will be equal to V G 1 minus V GS 1 and that will also be biased at a drain voltage of V D sat.

What about the size of M 4? We will size M 4 we will choose W over L of M 4 such that V G 1 is equal to V T plus 2 V D sat. So, I am going to write down the relationship for M 4.

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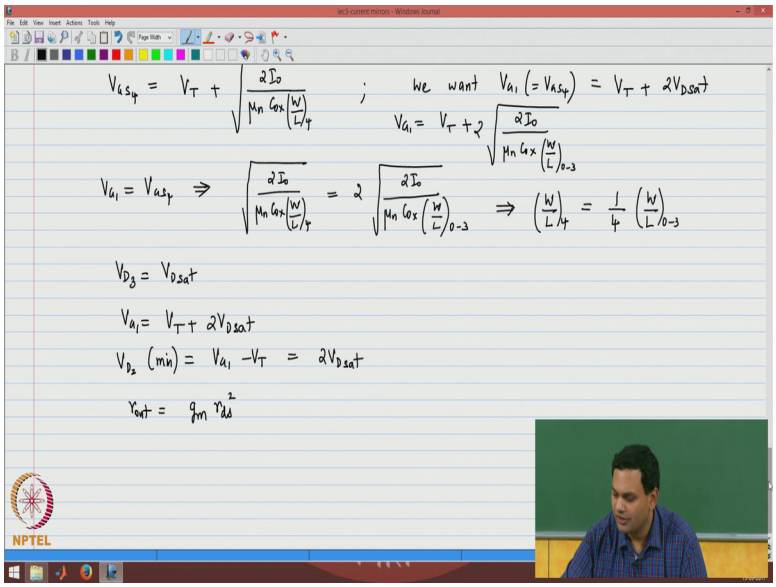

So, V GS 4 is note that M 4 also has a bias current of I naught this is the current voltage relationship for M 4 and note that we want V G 1 which is equal to V GS 4 please note that in the previous connection this voltage V G 1 is the same as V GS 4.

So, we want V GS 4, we want V G 1 to be V T plus 2 V D sat. And what is V G 1 V T plus this is the expression. So, now, if V G 1 is the same as V GS 4 I am sorry; I have missed a 2 number here this implies that this means that W over L of transistor 4 is going to be one-fourth the W over L of the other 4 transistors 0 to 3, now the design condition is clear.

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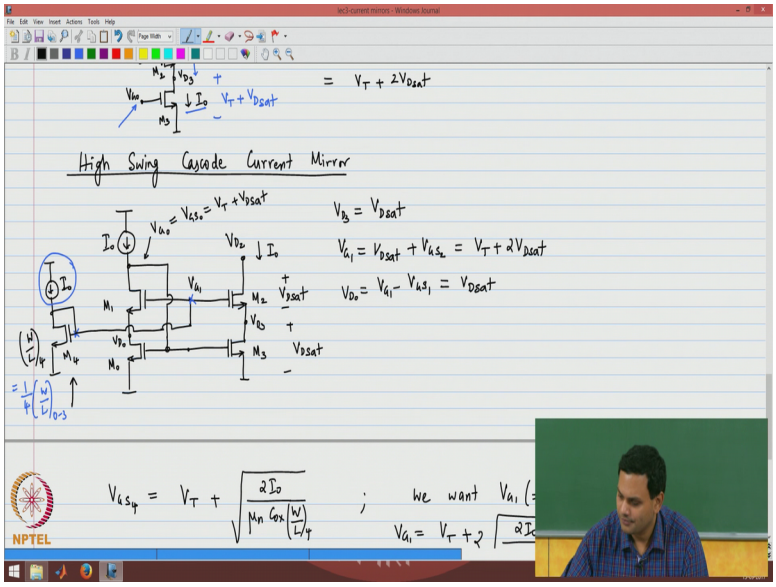

If you have a current I naught here, if you have a current I naught flowing through M 4 the size of M 4 should be one-fourth the size of the other 4 transistors if you do that the voltage generated at the gate of M 4 will be exactly equal to V T plus 2 V D sat. And if this is done V D 2 minimum in such a condition V D 3 will be equal to V D sat V G 1 is V T plus to V D sat. So, V D 2 minimum that is the minimum voltage possible at the drain of M 2 is 2 V D sat.

In other words you have now manage to bias the transistor such that each of these M 3 and M 2 has can have a voltage of only V D sat across it and still be in saturation and support the current I naught and finally, have an output resistance which is equal to gm r ds squared. So, this is a very commonly used current mirror it is called the high swing cascode current mirror.