Analog Integrated Circuits
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Lecture – 26
Telescopic OpAmp – I

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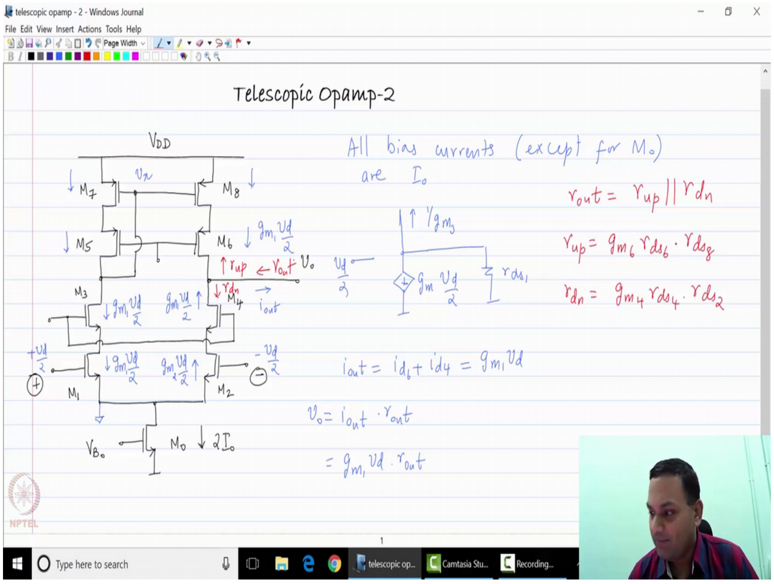

So, far we have seen the evolution of the telescopic opamp from the one stage regular one stage opamp. So, the really important things to note are that you replace the deflection pair, with cascode spare transistors. And you replace the upper current mirror by a cascode current mirror. So, in other words you create a cascode section for both the upper section and the lower sections.

Now, let us look at a very qualitative at a very high level let us look at what would happen in the circuit; when driven with differential signals and later we will move on to the small signal analysis. So, let us assume that I am applying voltage of plus V d by 2 and minus V d by 2 to the inputs of the opamp.

Now, as always I am going to assume that this common source node of M 1 and M 2 of the input pair is small signal ground this is of course, valid because the devices on both sides are highly identical. And the current through the transistors M 1 and M 2 is symmetrical. So, therefore, the bias current of course, splits equally between the 2 paths. So, all bias currents in the except for M naught are i naught. So, the bias current through which transistor in the circuit M 1 to M 8 is i naught. Of course, the current through M 0 is 2 i naught.

Now, since the common source node of M 1 and M 2 is a small signal ground, the current through M 1 is gm times V d by 2 downwards the current through M 2 is of course, gm times V d by 2 upwards; where gm is gm 1, and which is also equally to gm 2. Now what happens to this current. So, let us look at the current through the left half. So, if i look at this current, this current has 2 paths to flow. One is through the resistance of M 1 itself.

So, if i where to look at the current flowing gm times V d by 2, I am looking only at transistors M 1. So, this current can flow through 2 parts the first path is through r d s 1 itself. The second path is upwards into transistor M 3. For that i need to find out the impedance looking upwards in through the drain of into the source of M 3.

This impedance happens to be very close to 1 over gm 3. So, most of this current flows through transistor M 3. Therefore, we can say that this currents is gm 1 V d by 2. And so, is this current. Now what happens to the current through the left side? The current flowing through the left side flows through M 7 and M 5. So, both those currents are also gm 1 V d by 2 flowing downwards.

Now, this will generate a small signal voltage V x at this node, and that will cause a small signal currents to flow through M 8 and again that currents flows through M 6. And finally, flows through the into the output node. Now at the output node, at the output node the current flows out. Now this current since this circuits as no load the currents flow will flow through the overall output resistance at the output node.

As you can see the 2 currents flowing from M 6 and M 4 are in phase and will add at the output. So, i out is i d 6 plus i d 4. This is nothing but gm 1 times V d. So, the output voltages that is generated is i out, times r out. And r out is nothing but the impedance looking upwards and downwards. So, let us see what r out is r up. So, the impedance is looking upwards, and in parallel with the impedance looking downwards.

So, let us write down in red color is r up parallel r down. And r up is equal to gm 6 r d s 6 times r d s 8. And r down is gm 4, r d s 4 times r d s 2. So, you will have 2 cascode resistances. One cascode resistance looking upwards, which is the output resistance of the current mirror M 5 M 6 M 7 M 8 and you have the resistances looking downwards which is which is cascode resistance of M 2 and M 4.

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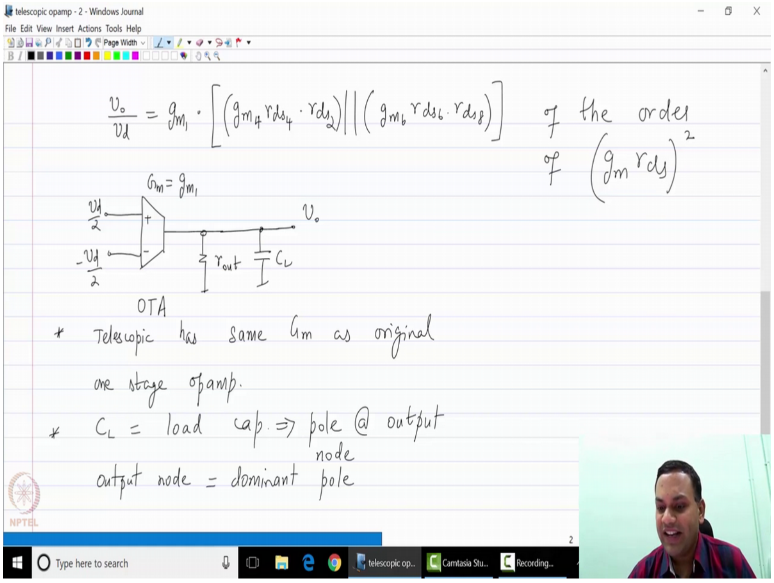

And therefore, the overall voltages gain is extremely large. So, V o by V d is the overall voltage gain of this circuits.

This is nothing but gm 1 times gm 4 r d s 4 times r d s 2, in parallel with gm 6 r d s 6 times r d s 8. So, this is the voltages gain of the circuits. This is clearly of the order of gm r d s the whole square because you have the product of 2 gms and the product of 2 g r d s.

So now we have got the you know gain from an d c gain from an opamp; that is of the order of the square of the intrinsic gain of a single amplifier. Now this is clearly much larger than the original one stage opamp. Now let us quickly point out couple of things. Now the if you look at the overall gm of this device. So, if you look at this opamp, this opamp is also best represented by an operational trans conductors amplifier. Because the it has a trans conductance and a very large output resistance. This is the output resistance, and the trans conductance is nothing but gm 1.

So, as you can see the trans conductance of the of the telescopic OTA. Telescopic OTA is the same as the trans conductance of the original one stage opamp. Is the same as the original one stage opamp. So, that is something very important. The other thing to note is that if you where to drive some load capacitance c l, you will now have a pole at the at the output node.

As we saw in the case of the one stage opamp, the output node was the dominant node, and same is expected to be the case here. So, the output node contributes the dominant pole. Now let us now that we have drawn the block diagram.

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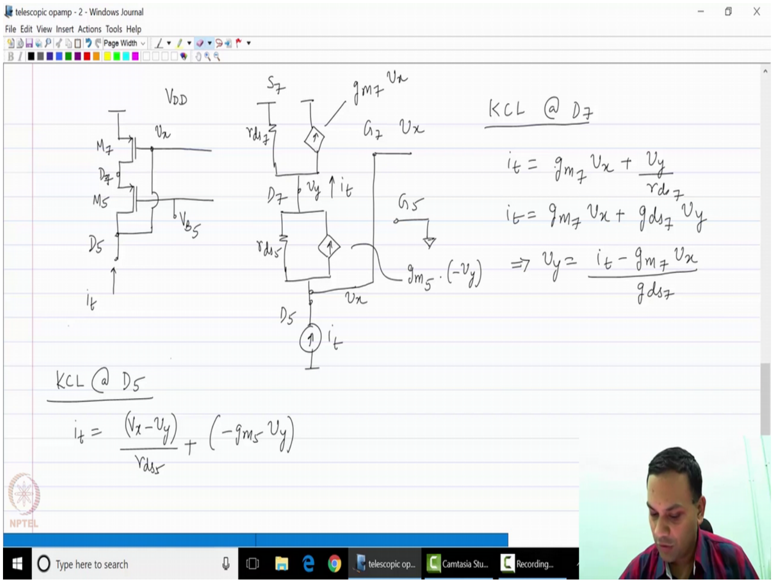

Let us now look at some of the details of this circuits. So now, let us quickly find out the output resistance of the portion looking upwards.

So, we want to find out what will happen, if you were to apply a current. I test going into this particular currents mirror. Because we want to find out what V x is generated at this node. So, if i where to excite this currents mirror with i test i want to find out what the input impedance of this particular structure is. So, let us drawn this small signal equivalence circuits of the left hand side portion alone. As you can see the right hand side portion will not come into the picture for small signal analysis for finding out the input resistance.

So, let us draw the small signal picture of the left hand side alone. And let us mark the nodes. So, this is drain 5, this is drain 7. I can now remove this portion of the circuits with no with nothing the circuits being excepted. So, let us do that. So, I am going to call this node D 5 this node D 7. So, clearly D 5 is the node which is being excited with my test currents source, this is D 7 and the gate of M 7; which is will call g 7 is also shorted to this particular node. And of course, the gate of M 5 was originally connected to some bias voltages V b 5 which we will now connect to ground.

The source of M 5, M 7 is connected to small signal ground, and the source of M 5 is the same as that in a M 7. So, let us now excite this with a test currents source i test and figure out what V x is V x is a same as V test, and that will tell us what the V x by i t will tell us what the input impedance of the circuits is. So, let us now write down the relevant equations for this particular circuits. So now, let us call this voltages V y. So, V x and V y need to be determined. So now, of course, this currents is gm 7 times V x and this currents is gm 5 times minus V y.

So now if you were to apply k c l at node D 7 you will find that the total current flowing up is again i t because the same currents i t splits into these 2 parts and combines to flow out into V y. So, i t is equal to gm 7 V y over r d s 7 and we will now write this as gm 7 V x plus gds 7 V y. So, this is our first equation. And from this we can say that V y is i t minus gm 7 V gm 7 V x over gds 7.

Next we will write k c l at D 5. Again we can say that i t is equal to V x minus V y over r d s 5 plus minus gm 5 V y. So, this is nothing. So, we will now rewrite this.

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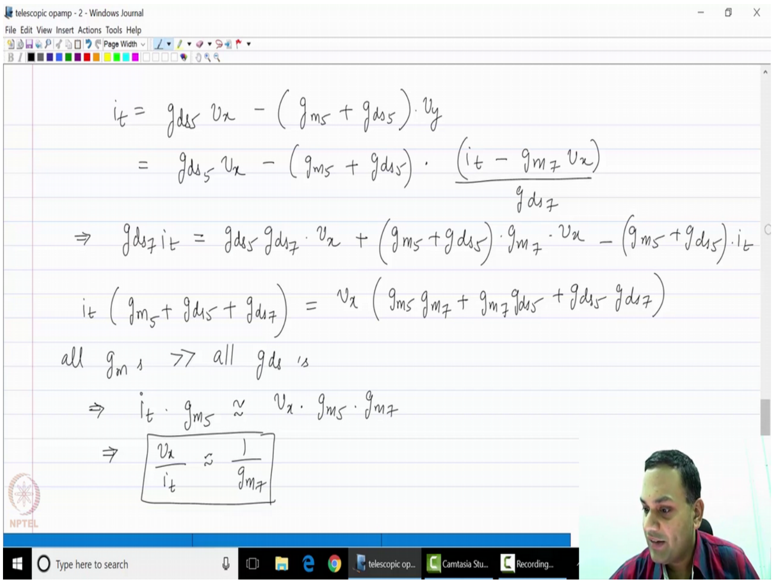

So, i test is gds 5 V x g d s 5 V x minus minus gm 5 plus gds 5 into V y. Now V y itself is i t minus gm 7 V x by gds 7.

Therefore we can say that gds 7 i t is equal to gds 5 V x, plus gm 7. I am sorry, gds 5 into gds 7 into V x plus gm 5 plus gds 5 into gm 7 into V x. And combining this term times this term to give me the second V x term. Finally, the third term is minus gm 5 plus gds 5 times i t.

Therefore i t times gm 5 plus gds 5 g plus gds 7 is equal to V x times gm 5 gm 7 gm 7 gds 5 plus gds 5 gds 7. Now we will now say that all gms are much much larger than all gdss. So, in other words we have saying that all the trans conductances are much larger than all the output conductances. So, if you apply this approximation i t times gm 5 is approximately equal to V x times gm 5 times gm 7. And this tells me that V x over i t is approximately equal to 1 over gm 7.

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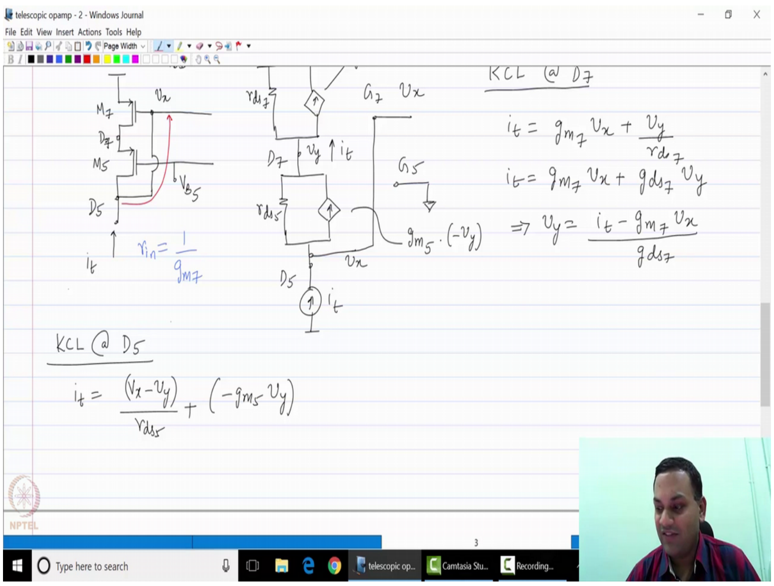

So, please note that the impedance looking upwards r out or r in is 1 over gm 7. Please note that this means that this indicates that there is inherent feedback by connecting the drain of M 5 to the gate of M 7.

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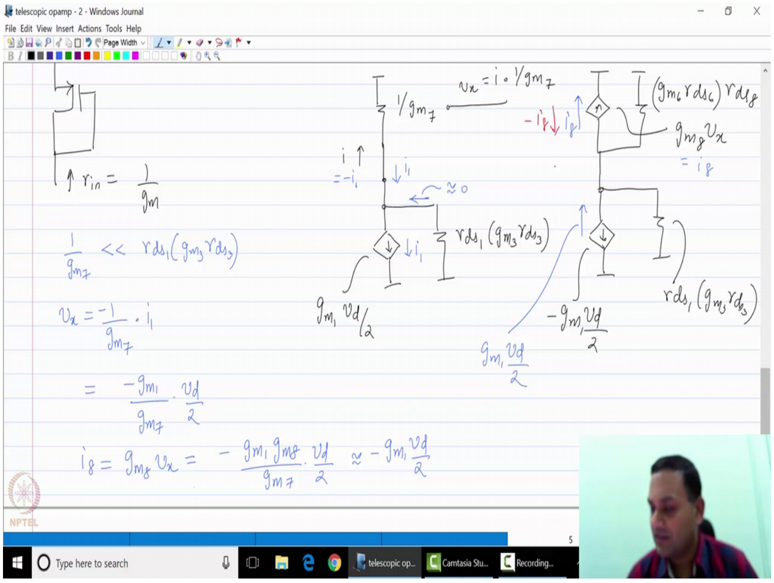

So, this is very similar to taking a common or taking transistor, and connecting it is own gate to it is source it is drain they r in for that 1 over gm. Now it turns out that even for a cascode currents mirror this feedback action gives you input impedance of 1 over gm 7.

So, this simplifies the equation alot for us. Because the small signal model can now be simplified in in a large manner. So, we will now draw the small signal equivalence circuits for the overall system. So now, the impedance looking upwards is simply 1 over gm, but i also create a voltage V x which is this currents let us call that i, i times 1 over gm.

So, remember that this V x is now connected to the note that this V x is now connected to the gate of M 8. And therefore, the currents through M 8 would be correspondingly gm times this voltages V x gm 8 times V x, this is rds 8. So now, let us complete the rest of the small signal picture while keeping this in mind. Now for the bottom portion of the circuits, we are now going to replace the cascode devices. So, signal equivalence the small signal equivalence of the cascode would be a trans conductors of value gm 1 times V d by 2. And a resistance looking out downwards which is rds 1; which is rds of 1 times gm rds of 3. And that is the output resistance of the cascode.

So, rds 1 into gm 3 r ds 3 similarly, on this side the circuits becomes this this is minus gm V d by 2 minus gm 1 V d by 2. And this resistance is again the same which is rds 1 into gm 3 rds 3. As you can see now the signal current, the direction is as follows this currents gm 1 V d by 2 as 2 pass to split the input resistance looking upwards is much much smaller than the input resistance looking downwards. In other words 1 over gm 7 is much much smaller than rds 1 into gm 3 rds 3.

Therefore if this currents where i 1 all of this currents i 1 flows upwards into M 7 and M 5. And that generates a voltage. So now, we can now write the write subscripts here the voltage V x is equal to 1 over gm 7 times i 1. And this is nothing but I am sorry and of course, the currents directions are downwards. So, let us use the correct current directions. So, that we do not make a mistake in the signs.

So, these currents and this currents has been pulled by i 1. So, i one flows through 1 over gm 7 this is approximately 0 because it is such a large output resistance. Now V x is now minus 1 over gm 7 into i 1. So, clearly so, i is equal to minus i 1, the x is minus gm 1 by gm 7 times V d by 2. Now the currents through M 2 is simply gm 1 V d by 2 flowing upwards.

Now, V x also generates a currents through M 8. So, let us call that i 8. Now i 8 is nothing but gm 8 times V x. So, this is nothing but minus gm 1 gm 8 by gm 7 times V d by 2. Since gm 8 is a same as gm 7 this is minus gm 1 V d by 2. And remember that i 8 flows upwards. Which means that is currents gm 1 V d by 2 flowing downwards into this problem. So, the currents flowing downwards is minus i 8; which is g M 1 V d by 2. So now, you have currents of M 2 which is flowing upwards which is gm 1 V d by 2 and currents of M 8 which is also flowing downwards into the same node.

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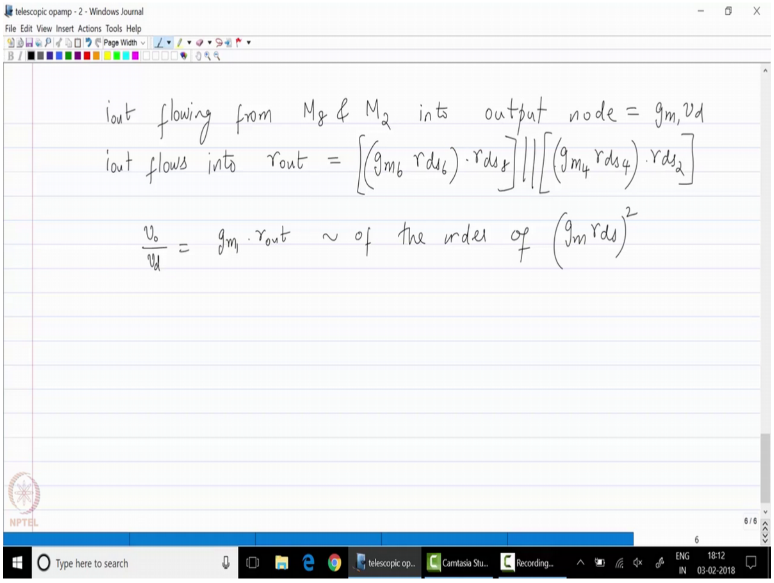

So, the total output currents r is nothing but the total output currents let us call that i out is minus i out from M 8 and M 2 into the output node this is equal to gm 1 times V d.

Now, what resistance do they flow through? Please note that this resistance is of course, is not rds 8, this is rds 8 into and this is the cascode resistance looking upwards which is rds 6, rds 6 gm 6 rds 6 times rds 8. So, this resistance is actually i 8 because we have drawn the simpler equivalence circuits of the upper cascode transistors. Now this currents i out flows into the output resistance of the overall opamp which is gm 6 rds 6 times (Refer Time: 28:23) looking and parallel with gm 3 rds 3 times rds 1 or gm 4 rds 4 times rds 2 looking downwards.

So, this output resistance of course, gets multiplied by i out to give you d out by V t to be equal to gm 1 times r out. So, this is the gain of the opamp clearly is of the order of of are the square of the intrinsic gain of one signal device.