Analog Integrated Circuits
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Lecture – 24
One-Stage OpAmp Example – 2

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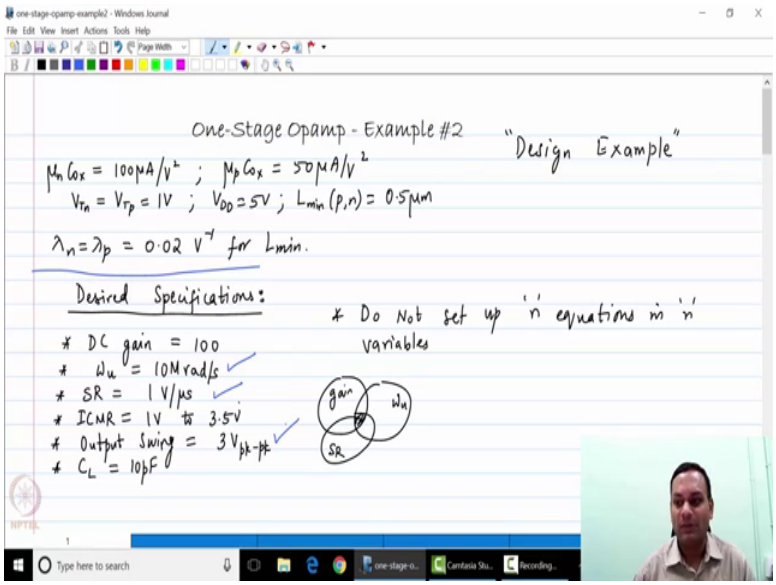

In this second example, we are going to try to approach the problem from the opposite angle. So, this is going to be design example. So, the previous example was an analysis example, where you were given the sizes and given the currents, you were asked to calculate what the parameters of the opamp were. In this case, we are going to pose the inverse problem, which is actually a tougher problem. So, we are going to give the list out the specifications of the opamp, and we are going to be asked to derive the sizes of the devices as well as the bias currents. So, we will use the same parameters that we had used before mu n C o x is 100 micro amp per volt squared, mu p C o x is 50 micro amp per volt squared. The threshold voltages V T n and V T p are both 1 volt. The power supply is 5 volts, the minimum length is 0.5 micrometers, and lambda n and lambda p for this minimum length is 0.02 volt inverse. So, these are the device parameters.

So, let us now list out the specifications. So, these are the desired specifications of the opamp. So, let us say that you need a DC gain of at least 100, and the unity gain frequency omega u should be equal to 1 or rather 10-mega radiance per second. The slew

rate of the opamp should be 1 volt per microsecond. The input common mode range should be between 1 volt to 3.5 volts; and the output swing should be 3 volts peak to peak. So, these are the minimum required.

So, if the DC gain is more than 100 that is fine. So, you need a minimum DC gain of hundred you need a minimum omega u of 10 mega radian per second, you need a minimum slew rate of 1 volt per microsecond. These are the required minimum input common mode range the common mode range can be wider if required. And finally, the output swing minimum swing required is 3 volt peak to peak.

Now, our job now is to translate these specifications into a set of widths and lengths and bias currents for the transistors. So, now let us start off listing out the requirement. So, first of all each of these parameters specifications that here required actually depends on certain variables such as g m, g d s capacitance etcetera. So, the one thing we need to we have not added is the load capacitance C L which we shall say is 10 picofarad. So, now, you can see that you have several sets of parameters. Now, it is very difficult so to set up equations in you know n equations in so many variables because very often there is no one unique solution. The number of constrains listed here are actually smaller than the number of degrees of freedom. So, there are actually many solutions. So, we will try to approach it in a somewhat of a logical manner where we can try to set some of the parameters first.

So, the first thing to do is so do not set up n equation in n variables and solve it that is not the way to go around, because you have several parameters suggest gain, omega u, slew rate etcetera, and it turns out that there may actually be no one unique solution. So, we need to be little bit careful. And finally, please note that in this particular case, there are other specifications that I have not given such as noise, offset or power consumption. So, let us try to approach this in a different manner. So, first we will write down the dependence of each of these parameters. Now, it is logical for us to start with the parameters that depend only on one variable. So, let us look at which those parameters are.

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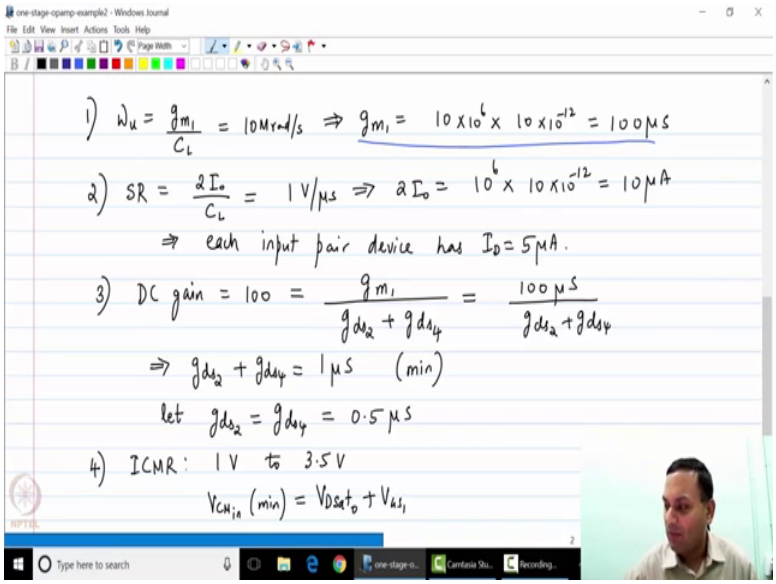

So, clearly those two parameters are omega u and the slew rate. So, let us start from there. So, omega u is nothing but g m 1 over C L where g m 1 stands for the transconductance of the input pair. So, this should be equal to 10 mega radiance per second. This means that g m 1 should be equal to 10 into 10 power 6 times 10 into 10 power 10 power minus 12 or 100 microsiemens. So, this now is a good place to start because this let us set the value of the g m of the input pair, which is one of the most important parameters in your design.

Now, let us look at the slew rate specification. So, the slew rate specification depends only on the total bias current which I will denote by 2 I naught over C L. And this is supposed to be 1 volt per microsecond, so which means 2 I naught is 10 power 6 times 10 into 10 power minus 12 or 19 microamperes. This means that each transistor input pair has a 5 microamp bias current. Now, it turns out that all of the other parameters depend on many other variables, but let us look at now look at them one by one.

The DC gain. So, it is one, number two. The third parameter will look at is the DC gain and the DC gain is suppose to be 100, this is nothing but g m of the input pair over the sum of the g d s 2 at the g d s s of the output pair. Since, we have already found out g m 1 here, we will plug that in here. So, this is 100 microsiemens over g d s 2 plus g d s 4. And now this tells us that g d s 2 plus g d s 4 should be equal to 1 microsiemen. Now, we will now make a judgment call and this is one of the parts of design is to instead of

setting up equations in variables, we will now make a judgment call and say let the two resistances or two conductances be equal. Let g d s 2 be equal to g d s 4 be equal to point 5 microsiemens. So, please note that this is the minimum g d s 2 required; if g d s 2 were smaller than this then the DC gain would be larger. The important condition is that the sum of the g d s 2 should be larger than 1 microsiemen.

Now, let us look at the input common mode range spec, the input common mode range says that the input common mode should be variable between 1 volt and 3.5 volts. What does this tell us if please remember that for a for the one-stage opamp we have seen so far, the minimum input common mode is equal to V D sat of m 0 which is the current source plus V GS of the input transistor. Now, clearly the threshold voltage of the device is already 1 volt.

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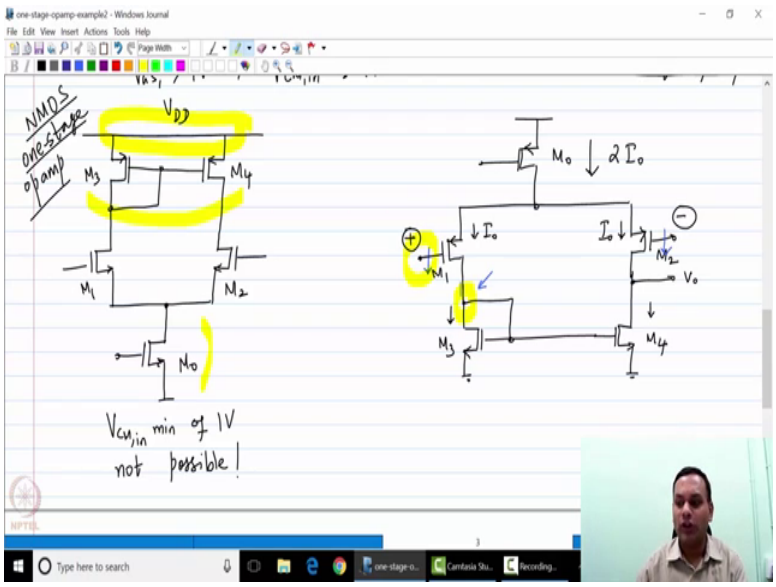

We now have a problem because V GS 1 should already be larger than 1 volt V m in has to be large than 1 volt for the opamp that we have seen so far; M 0, M 1, M 2, M 3 and M 4. Now, clearly for the opamp we have seen so far the minimum input common mode is the point where M 0 goes to the edge of triode region where this is V D sat and you need a minimum V GS 1 across the gate source of M 1. Now, clearly a minimum input common mode level of 1 volt is not possible for this opamp. So, however, please note that this is not the only one-stage opamp possible as we have seen the NMOS device and the PMOS device have identical small signal pictures which means you should be able to

interchange the NMOS and PMOS transistors, and be able to get circuit with the exact same small setting characteristics. The only difference being that the bias points would be different.

So, let us now look at the PMOS one-stage opamp. So, far we have been looking at the NMOS one-stage opamp; clearly that will not work in this particular design example. So, let us build the PMOS one-stage opamp. So, in the case of the NMOS opamp, you had a transistor M 0 that produced that acted as the current source. So, now you need a PMOS transistor M 0 that would act as a current source, pumping current of 2 I naught into the differential pair. Now, this particular circuit will also have a PMOS input pair. And let us say this is the positive input and this is the negative input. And now the PMOS current mirror here would be replaced with an NMOS current mirror

And now these transistors are M 1, M 2, M 3 and M 4. The sources of the NMOS current mirror is connected to ground analog us to the connection to V DD for M 3 and so on. Now, it turns out that all the equations we have written are valid for this particular opamp also, since we have not gone from the small signal parameters g m and g d s 2, the bias points I d and mu C o x etcetera. So, now let us look at the minimum input common mode range of this particular opamp.

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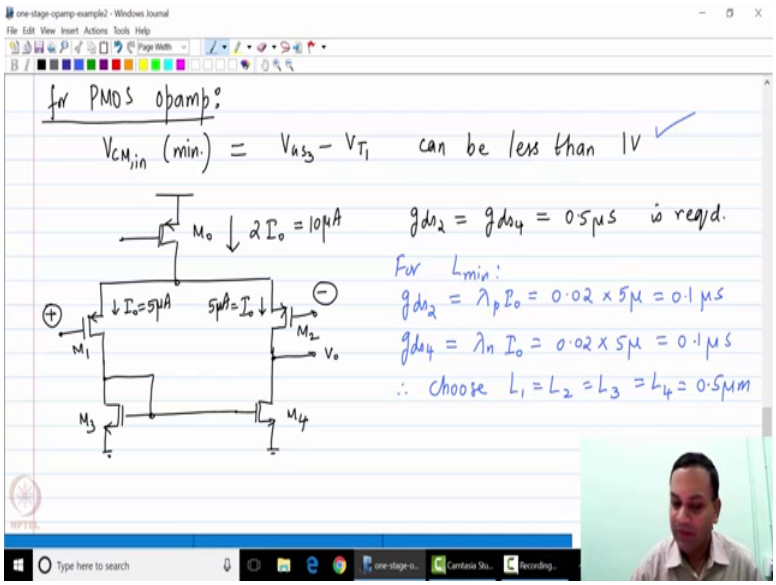

So, we are now going to look at the PMOS opamp. So, for the PMOS opamp all the equations are valid, but we are specifically interested in the input common mode. So, if I

were to start reducing the input common mode, I can see that this particular voltage is constant because there is a current of I naught through each of these passive devices M 1 and M 2, and M 3 and M 4. And the output of course, is taken at the drain of M 4. And you can see that this node has a constant voltage of V GS 3. And the gate of M 1 can go lower than this node by a value by a voltage equal to the threshold voltage of the PMOS transistor which is V T 1 or V T P. Now, clearly this can be less than 1 volt if required by choosing V GS 3 appropriately. Now, it is clear that the PMOS opamp is the circuit that we need to use in this case.

So, now, let us continue with the PMOS version of the circuit. So, now for this circuit, we now know that 2 I naught is equal to 10 microamps, and therefore each transistor has a bias current of 5 microamps. Now, based on this, we can now calculate the W over L etcetera. So, let us now come back from the expression for g d s 2 and g d s 4, because the minute you know the bias current you can calculate the value of the length of the device. So, as you can see g d s 2 is equal to g d s 4 is equal to 0.5 microsiemens.

Now, we are given that the lambda for L min of 0.5 micron is 0.02 volt inverse. So, let us assume that l is equal to L min and find out what the value of g d s 2 and g d s 4 is. So, for our circuit, if we were to use L min g d s 2 is lambda p times I naught, this is 0.02 times I naught is 5 microamps or 0.1 microsiemens. Similarly, g d s 4 is lambda n I naught which is again 0.02 into 5 microamp which is 0.1 microsiemens. It is clear that in this particular case an L min already gives you a larger value of r d s 2 and a smaller value of g d s 2 and g d s 4 then as required. So, clearly g d s 2 of 0.1 microsiemens and g d s 4 of 0.1 microsiemen is more than enough. With these values, we decide that L 1 is equal to L 2 is equal to L 3 is equal to L 4 equals 0.5 micrometers. If the value of output resistance was large enough if g d s 2 and g d s 4 were not small enough, you would have to increase the length of the transistor to get a larger output resistance. In this particular example, this is good enough.

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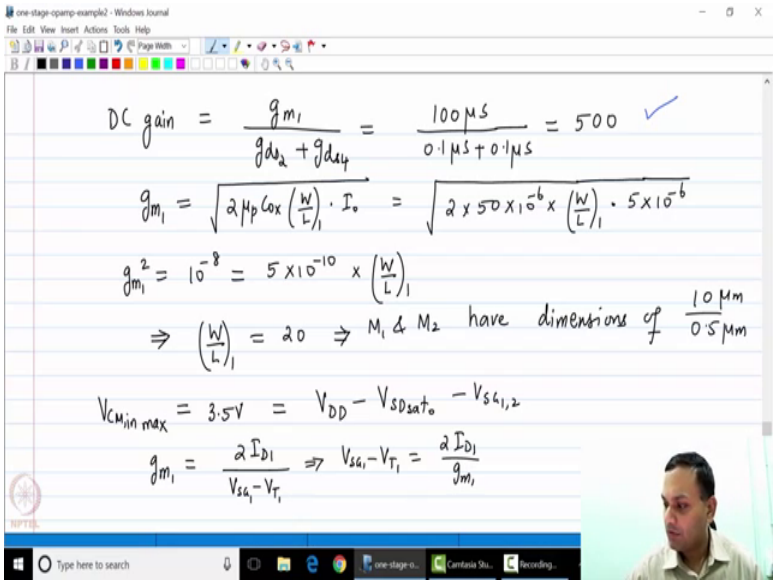

Now, you can see that the DC gain is now larger than expected DC gain is g m 1 by g d s 2 by g d s 2 plus g d s 4. As we have seen earlier, the value of g m 1 was determined to be 100 microsiemens. So, therefore, the DC gain is 100 microsiemen over 0.1 microsiemen plus 0.5 microsiemen, which is 500 volts per volts. We wanted a minimum gain of 100, but we now have a larger DC gain than required which is always better. So, this the DC gain spec is met.

Now, the next thing to do is to calculate the width to length ratio of M 1 and M 2. Now, g m 1 is nothing but root of 2 mu C o x to 2 mu p C o x W over L of one times I naught this is nothing but root of 15 10 power minus 6 W over L of 1 times 6. Therefore, you can see since g m 1 is 100 microsiemen, g m 1 squared is 10 power minus 8, this is equal to 5 into 10 power minus 10 into W over L of 1. This means that the width to length ratio of transistor one is 20 or so this means M 1 and M 2 have dimensions of 10 over 0.5, so 10 micron over 0.5 micron.

So, now have the sizes of M 1 and M 2, let us now decide the size of M 0. Since we know the size of M 2, we can now calculate the value of the size of M 0 in the following way. So, we know that V CM in max should be equal to 3.5 volts. We know that V SG this should be equal to V CM in max is equal to V DD minus V SD sat 0 minus V SG 1, 2 because the maximum input common mode happens when you have exactly V SD sat across M 0. And therefore, the common mode at the input will be exactly V DD minus V

SD sat 0 minus V SG of 1. Now, V SG 1 is given by the following relationships, it should be V T plus. So, let us calculate it in a different way this time. So, let us calculate it from the g m, g m 1 is 2 I D 1 over g 1 minus V T 1. So, let us calculate it from this expression, this means that V SG 1 minus V T 1 is 2 I D 1 over g m 1.

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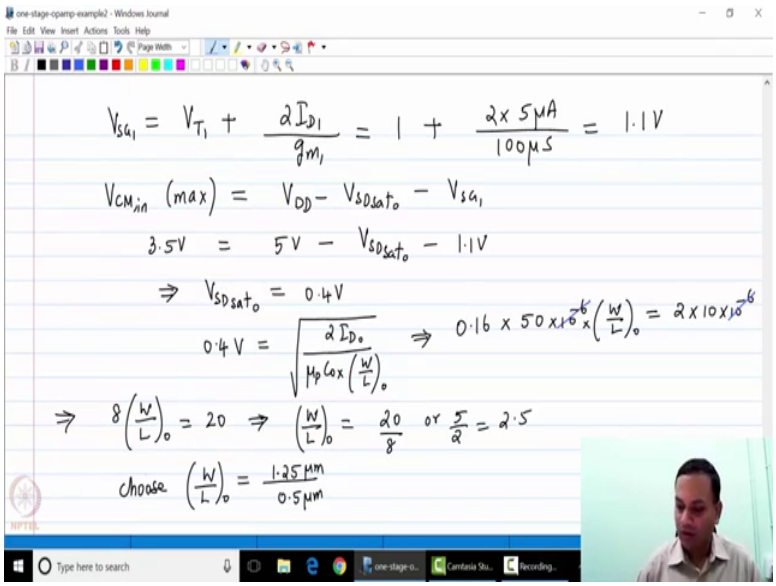

So, V SG 1 is V T 1 plus 2 I D 1 over g m 1 V T 1 is 1 volt plus the current through M 1 is 5 microamperes and g m 1 is 100 microsiemens. And therefore, this is nothing but 10 microamp over 100 microsiemens this is 1.1 volt in such a case the value of V CM in max which is 3.5 volts. So, let us write that down here again is V DD minus V SD sat 0 minus V SG 1. So, 3.5 volts is 5 volts minus V SD sat 0 minus 1.1 volt tells us that V SD sat zero has to be equal to 0.4 volts.

Now, since we know the current through M 0, we can now calculate the width to length ratio of M 0 itself. So, V SD sat 0, so 0.4 volts is equal to 2 I d 0 over mu p C o x W over L of 0.16 into 50 into 10 power minus 6 into W over L 0 is equal to 2 into 10 into 10 power minus 6, because the current through M 0 is 10 microamps. So, 8 times W over L of 0 is equal to 20. So, 50 times 0.16 is 8. So, 8 times W over L of 0 is equal to 20, this means that W over L of 0 is equal to 20 by 8 or 5 by 2 or 2.5. So, therefore, we choose W over L of 0, we know that the easiest choice is to choose a 0.5 micron length for M 0 because as of now there is no CMRR spec. And the size of the width is now simply 2.5 times 0.5, which is 1.25 micrometers.

So, now we have now selected the sizes of these transistors, we have selected the sizes of M 0, we have selected the sizes of M 1 and M .2 And now we need to decide the size of M 3 and M 4. As we will go back to the spec, we will find that there is one more spec that we have not used, which is the output swing specification that will set the size of M 3 and M 4.

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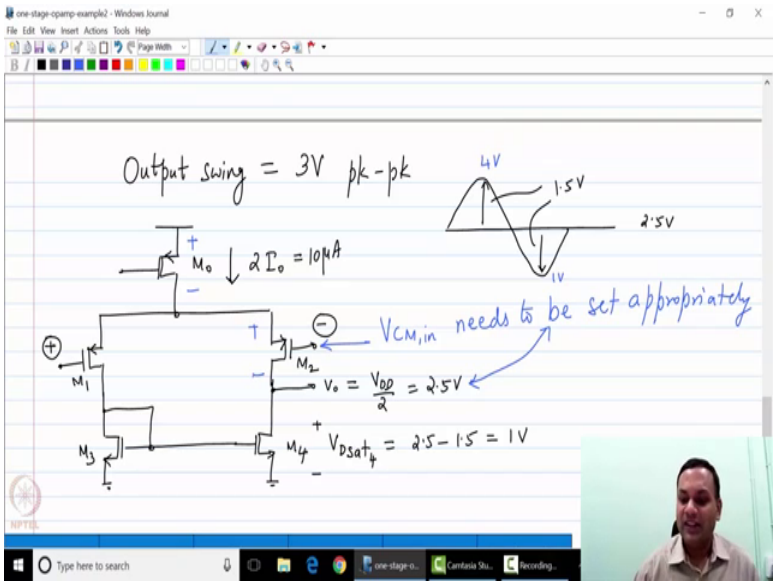

The minimum output swing is 3 volts peak to peak. So, let us assume that this swing is equally distributed on the upper side and the lower side. So, let us depict it on this particular picture. We will assume that feedback is used to set V 0 to be equal to V DD by 2 or 2.5 volts, which is a fairly good estimate which is a fairly good place to bias the opamp. Now, on top of this 2.5 volts, we now want a 3 volt peak to peak swing which means the amplitude is 1.5 volts. And at that point the transistors on either side should just as that touch the triode region, this tells us that the V D sat of M 4 should be equal to 2.5 minus 1.5 equals 1 volt. This now sets the size of M 4. Let us now calculate that.

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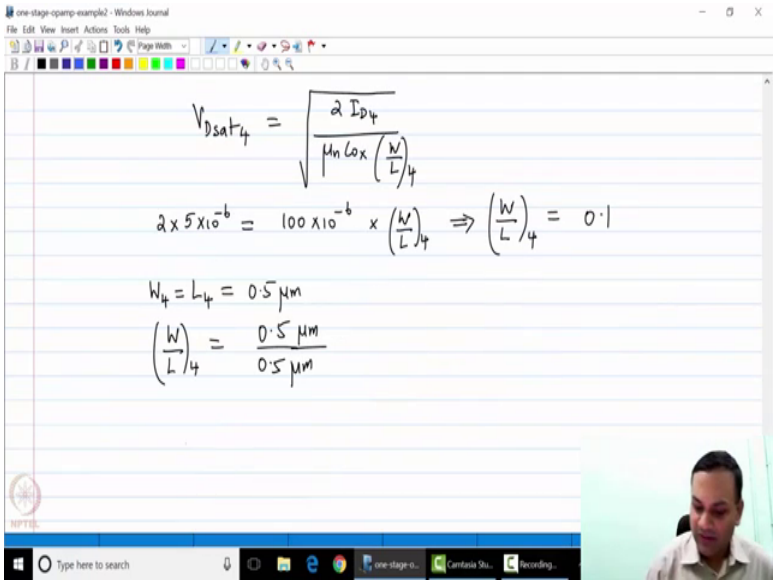

So, V D sat 4 is simply 2 I D 4 over mu n C o x W L 4. And since this is equal to 1, we will square both sides and point out that 2 into I D 4 is 5 microamps should be equal to mu n C o x which is 100 microamp per volt squared times W over L of 4. Now, as you can see W over L of four needs to be 0.1, but clearly a width of which is smaller than the length is normally not possible and therefore, we will say that W 4 is equal to L 4 is equal to 0.5 micrometers. So, we will say that this value is one in which case V D sat is even lower than required.

Finally, we have to ensure for this to be correct we have to ensure that if V naught needs to be easily biased at 2.5 V CM in needs to be biased appropriately, so that the output can be set to 2.5 volts. And as we have seen the maximum output voltage just like we said that the minimum output voltage is 1 volt, the maximum output voltage is 4 volts. In which case the common mode at the input needs to be set such that the sum of these two voltages with the other polarity of course, because we have a PMOS opamp. So, the sum of these two voltages at the edge of triode regions should be equal to one volt. Let us quickly check if that is true.

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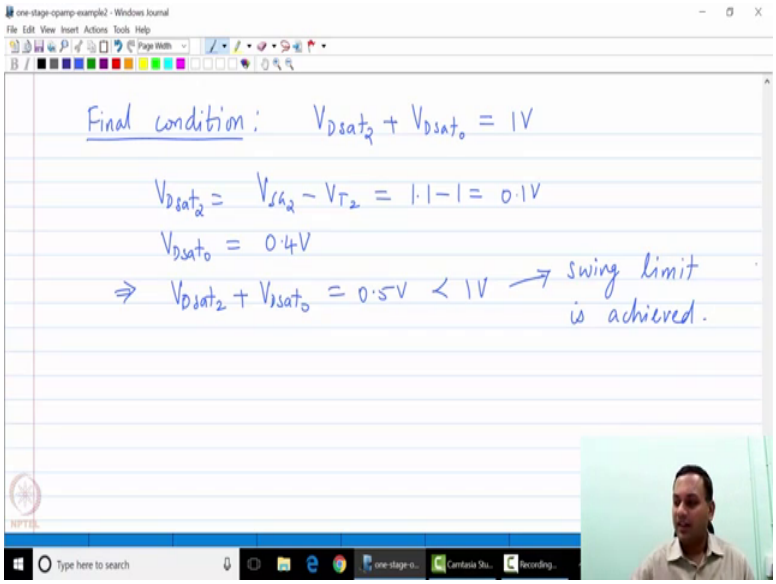

The final condition is that V D sat of M 2 plus V D sat plus V D sat of M 0 should be equal to 1 volt. Let us check if this is true V D sat 2. So, we have seen that V SG 1 is 1.1 volts. So, which is the same as V SG 2 and V SD sat 0 is here which is 0.4 volts by design clearly V D sat 2 plus V D sat 0 is 0.5 volts which is less than 1 volts swing limit is achieved. Please note for this final swing limit condition that we have applied at the end, I have assumed that the gain of the amplifier is so large that for the triode condition, I can neglect the gains neglect the swings at the gate. So, please note this, for a hand calculation this is often perfectly fine as long as the gain of the amplifier is very larger. In this case, our DC gain 500, so therefore, we have no problems with neglecting the swings at M 1 and M 2 gates.