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Lecture – 23
One-Stage Op Amp Example - I

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The image shows a handwritten slide titled "One-Stage Opamp - Example #1". It contains a circuit diagram of a differential pair with a current mirror load and a tail current source. The circuit is powered by a 5V supply (V_{DD}) and a 2V supply (V_{DD0}). The output is taken from the differential pair and drives a load capacitor C_L = 100pF. The circuit parameters are: μ_nC_{ox} = 100 μA/V², μ_pC_{ox} = 50 μA/V², V_{Tn} = V_{Tp} = 1V, V_{DD} = 5V, L_{min}(p,n) = 0.5 μm, and λ_n = λ_p = 0.02 V⁻¹ for L_{min}.

The calculations shown are:

$$I_{D_0} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_0 (V_{B_0} - V_{Tn})^2$$

$$= \frac{1}{2} \times 100 \frac{\mu A}{V^2} \times \frac{10}{0.5} \times (2-1)^2 = 1 mA$$

$$I_{D_1} = I_{D_2} = 0.5 mA$$

$$g_{m1} = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right)_1 \times I_{D_1}} = \sqrt{2 \times 100 \mu A/V^2 \times \frac{20}{0.5} \times 0.5 \times 10^{-3}}$$

$$= \sqrt{4 \times 10^{-4}} = 2 mS$$

In this lecture, we look at a quick example to analyze the one-stage opamp that we have been looking at so far and we will try to put together as many of the datasheet components as possible, datasheet values as possible. So, to start off with this is the one-stage opamp, let us say that the opamp is driving a load capacitance of 100 picofarad. And let us also say that the device parameters are as follows μ_n c ox is 100 microamps per volts square, μ_p c ox is 50 microamp per volt square. Let us say that V_{Tn} is equal V_{Tp} is equal to 1 volt, and let us say that the supply voltage is 5 volts. And let us say that the minimum length possible for the PMOS and NMOS is 0.5 microns and lambda_n and lambda_p is equal to 0.02 volt inverse for 1 min. Let us start off with these numbers.

And let us say that the sizes of the transistors are as follows. So, m naught has a size of 10 over 0.5, all widths and lengths being in micrometers the width over length of M₁ is 20 over 0.5; M₃ and M₄ have a width over length of 40 over 0.5. And finally, let us say that V_B naught was equal to 2 volts. So, the first thing we can do is write down the expression for the voltages and currents of every device that we can we can analyze

Now, the first thing we will do is to find out the value of the current through M_0 which is I_{D0} . So, the current is as follows I_{D0} is half $\mu_n C_{ox} W/L_0$, I will do $V_{B0} - V_{Tn}$ the whole squared. And this is clearly half into 100 micro amp per whole squared times 10 over 0.5 into 2 minus 1 the whole square. So, this current through M_0 is equal to 1. So, this current is milliamperes. So, now, all the derived quantities will be placed in blue color. Now, of course, if that happens as long as both M_1 and M_2 are in saturation, you will find that each of them has a current, which is equal to half a milliamperes.

So, I_{D1} is equal to I_{D2} is equal to 0.5 milliamperes. So, you have a current of 0.5 milliamperes flowing through each of these half circuits. Based on this we can calculate the value of the g_m s of the different transistors. So, let us calculate the value of g_{m1} , g_{m1} is root of 2 $\mu_n C_{ox} W/L_1$ into I_{D1} , this is 2 into 100 micro into 20 by 0.5 into 0.5 e minus 3. So, this is clearly if I have to make the actions, so 0.5 and this is root of 4 into 10 power minus 6 which is 2 millisiemens. So, g_{m1} is equal to g_{m2} is equal to 2 millisiemens.

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The screenshot shows a Windows Journal window with the following handwritten derivations:

$$g_{m4} = \sqrt{2 \times 50 \times 10^{-6} \times \frac{40}{0.5} \times 0.5 \times 10^{-3}} = \sqrt{4 \times 10^{-6}} = 2 \text{ mS}$$

$$g_{ds2} = \lambda_n I_{D2} = 0.02 \text{ V}^{-1} \times 0.5 \text{ mA} = 10 \mu\text{S}$$

$$g_{ds4} = \lambda_p I_{D4} = 10 \mu\text{S}$$

1) DC (low-freq) gain = $\frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2 \text{ mS}}{10 \mu\text{S} + 10 \mu\text{S}} = 100 \text{ V/V}$

2) UHF $\omega_u = \frac{g_{m1}}{C_L} = \frac{2 \text{ mS}}{100 \text{ pF}} = \frac{2 \times 10^{-3}}{10^{-10}} = 20 \text{ M rad/s}$
 $f_u = \omega_u / 2\pi$

3) Slew rate (ave & -ve) = $\frac{I_{D0}}{C_L} = \frac{1 \text{ mA}}{100 \text{ pF}} = \frac{10^{-3}}{10^{-10}} = 10^7 \text{ V/s}$

Let us now calculate what the value of g_{m3} and g_{m4} is; g_{m3} or g_{m4} is root of 2 into $\mu_p C_{ox} W/L$, so which is 50 e minus 6 into the W/L of the PMOS transistors is 40 over 0.5 into 0.5 into 10 power minus 3. And this is clearly so 0.5 and 0.5 get cancelled and so this is root of 4 into 10 power minus 6, so this is also 2 millisiemens.

Once we know these two numbers, we know the transconductance of the devices. Now, we let us calculate the output conductance of the devices g_{ds2} is $\lambda_n I_{D2}$. So, this is 0.02 into I_{D2} which is 0.5 milliamperes, and this is 10 microsiemens. Similarly, g_{ds4} is $\lambda_p I_{D4}$; this is also 10 microsiemens.

Now, we are in a position to start writing down the expressions for the various datasheet components of the opamp. So, the first component that we will write down is the DC also call the low frequency gain of the opamp this is nothing but g_{m1} over g_{ds2} plus g_{ds4} . 1 over g_{ds2} plus g_{ds4} is nothing but r_{ds2} parallel r_{ds4} , so this is 2 millisiemens over 10 microsiemens plus 10 microsiemens. So, this is a gain of 100 volt per volt. So, this is the DC gain of the opamp.

The second component we will look at is the unity gain frequency of the opamp. So, ω_u is nothing but g_{m1} over C_L this is 2 millisiemens over 100 picofarad. So, this is 2 into 10 power minus 3 over 10 power minus 10 , so this is 20 mega radian per second. Of course, f_u is ω_u over 2π . The third component that we will write down, we will skip then dominant and non-dominant poles and zeros, because we do not know what the capacitance is at node x . Since, we are not given anything there we will assume that C_L is the only capacitance of interest.

So, the next component that we can write down is the slew rate. So, the positive and negative slew rate are both equal for the one-stage opamp is nothing but I_{D0} which is the maximum current that can flow in and out of the opamp over C_L . So, this is 1 milliamp over 100 picofarad. This is it is 10 power minus 3 over, so this is 10 power minus 3 10 power minus 10 or 10 power 7 volts per second.

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4) Input CM range

$$V_{CM(in) (min)} = V_{GS1} + V_{DSAT0}$$

$$V_{DSAT0} = V_{GS0} - V_{TN} = 2 - 1 = 1V$$

$$V_{GS1} = V_{TN} + \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_1}} = 1 + \sqrt{\frac{2 \times 0.5 \times 10^{-3}}{100 \times 10^{-6} \times \frac{20}{0.5}}} = 1 + \sqrt{\frac{1}{4}} = 1.5V$$

$$V_{CM(in) (min)} = 1.5 + 1 = 2.5V$$

$$V_{CM(in) (max)} = V_{DD} - V_{SD3} + V_{TN}$$

$$V_{SD3} = V_{TP} + \sqrt{\frac{2I_{D3}}{\mu_p C_{ox} \left(\frac{W}{L}\right)_3}} = 1 + \sqrt{\frac{2 \times 0.5 \times 10^{-3}}{50 \times 10^{-6} \times \frac{40}{0.5}}} = 1.5V$$

Next, we will write down the input common mode range. So, the minimum value of minimum is nothing but V_{GS1} . So, remember quick reminder, so when the input common mode is minimum, so as you keep decreasing the input common mode M_1 continues to have V_{GS1} across its gate source, and the same with M_2 , and the voltage at the common source node starts keeps falling with the decrease in common mode.

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One-Stage Opamp - Example #1

$\mu_n C_{ox} = 100 \mu A/V^2$; $\mu_p C_{ox} = 50 \mu A/V^2$
 $V_{TN} = V_{TP} = 1V$; $V_{DD} = 5V$; $L_{min}(p,n) = 0.5 \mu m$
 $\lambda_n = \lambda_p = 0.02 V^{-1}$ for L_{min} .

$I_{D1} = I_{D2} = 0.5 mA$
 $g_{m1} = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right)_1 \times I_{D1}} = \sqrt{2 \times 100 \times 10^{-4} \times \frac{20}{0.5} \times 0.5 \times 10^{-3}}$

And finally, M_0 is at the edge of triode and therefore, the input common mode level at that point should be V_{GS1} plus V_{DSAT0} . Now, V_{DSAT0} is V_{GS0} minus V_T . So, this

is 2 minus 1 which is 1 volt; and V_{GS1} is given by V_T , $V_T n$ plus root of $2 I_{D1} \mu C_{ox} W$ over L_1 . So, this is 1 plus square root of 2 into 0.5 into 10 power minus 3 over μC_{ox} is 100 into 10 power minus 6 into so the width to length ratio of M_1 and M_2 is 20 over 0.5. So, this is nothing but 1 plus square root of so this is 10 power minus 3, and this is 40 over 1. So, this is 1 over 4 or 1.5 volts. So, V_{GS1} is 1.5 volts, and therefore, the input minimum common mode is 2.5 volts.

What about the maximum input common mode? As we have seen before as we start increasing the input common mode, the gate of M_1 increases, but the drain of M_1 stays constant at V_{DD} minus V_{SG3} . And therefore, the limit is given by the point when M_1 just goes into triode region that happens at a voltage V_{DD} minus V_{SG3} , this is the voltage at the drain, the gate can go one threshold voltage of the drain. Now, let us calculate what V_{SG3} is so V_{SG3} is V_{Tp} plus root of $2 I_{D3}$ over $\mu p C_{ox} W$ over L_3 . So, this is 1 plus root of 2 into 0.5 into 10 power minus 3 over 50 into 10 power minus 6 into 40 over 0.5 or into 80, and as it turns out this is also equal to 1.5 volts.

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Handwritten notes on a digital whiteboard showing calculations for input common mode range and output common mode range.

$$V_{CM,in} (max) = 5 - 1.5 + 1 = 4.5V$$

$$ICMR = \{2.5V, 4.5\}$$

5) Output CM range

$$V_{OCM} (max) = V_{DD} - V_{SDsat4} = 5V - (V_{SA4} - V_{T4}) = 5 - (1.5 - 1)$$

$$= 4.5V$$

$$V_{OCM} (min) = V_{CM,in} - V_{T4} = V_{CM,in} - 1V$$

6) Input referred noise of the opamp

$$\bar{e}_n^2 = \frac{16kT}{3g_{m1}} \left[1 + \frac{g_{m3}}{g_{m1}} \right]$$

$$g_{m3} = g_{m1} = 2mS$$

Therefore, the maximum input common mode is given by 5 minus 1.5 plus 1 or 2.5 volts. So, the input common mode can be anywhere between 2.5 volts and 4.5 volts. So, this is the input common mode range. What about the output common mode range? So, the output common mode range can be calculated as follows. So, the maximum output common mode is given by V_{DD} minus $V_{SD sat}$ of 4. As we have seen V_{SG3} is 1.5

volts, therefore which is the same as V_{SG4} ; therefore, $V_{SD sat 4}$ is V_{SG4} minus V_{T4} , this is 5 minus 1.5 minus 1 or 4.5 volts.

Of course, the minimum output common mode depends on the value of the input common mode, so that would happen when as the output common mode decreases, eventually the transistor M_2 would go into triode region. And therefore, that will happen when the drain voltage goes one threshold voltage below the gate. So, this would happen $V_{CM in}$ minus V_{T4} , this is $V_{CM in}$ minus 1 volt.

Now, the next quantity that we will calculate is the input referred noise of the opamp. As we have seen before the input referred noise of the opamp so which we will represent as e_n squared, this has two components. So, this is $16kT$ by $3g_{m1}$ into 1 plus g_{m3} by g_{m1} . The first quantity the first portion represents the noise of the input transistors referred back to the input of the opamp. The second quantity this quantity represents the noise of M_3 and M_4 referred back to the input. As you can see the noise of M_3 and M_4 depend on g_{m3} , but the overall trans-conductance of the opamp depends on g_{m1} and therefore, the input referred component depends on both of these. As we have seen the since g_{m3} is equal to g_{m1} is equal to 2 milli Siemens.

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Handwritten notes and calculations:

$$\frac{e_n^2}{\Delta f} = \frac{16kT}{3g_{m1}} \times 2 = 2.208 \times 10^{-17} \frac{V^2}{Hz}$$

$$\frac{e_n}{\sqrt{\Delta f}} = 4.7 \frac{nV}{\sqrt{Hz}}$$

What is left?

- * Mismatch \rightarrow Offset voltage
- * $C_x \rightarrow$ Non-dominant poles & zeroes
- * CMRR $\rightarrow 1 + 2g_{mR_o} = 1 + 2g_{m1}r_{dso}$

$$r_{dso} = \frac{1}{\lambda_n I_{D_o}} = \frac{1}{0.02 \times 1mA} = 50k\Omega$$

$$\Rightarrow CMRR = 1 + 2 \times 2mS \times 50k\Omega = 201$$

Therefore, e_n squared is g_{m1} into 2 , and this happens to be equal to 2.208 into 10 power minus 17 volt square per hertz of course, we at always talking about the noise squared voltage density. So, I will make that explicit here. Finally, so the noise voltage

density, which is $e n$ over root delta f happens to be equal to 4.7 nano volt per volt hertz. So, this is the input referred noise density of the opamp. If you knew the mismatch characteristics, you could also calculate the mismatch characteristics. So, those there are two things that we have left uncharacterized. So, those are mismatch and calculation of offset voltage. Since, we did not specify a V_T mismatch, we have not calculated the offset voltage. And of course, we had not specified the capacitance at node x, and this would allow us to calculate the non-dominant poles and zeroes of the system.

Finally, there are two more things to wrap up this analysis. So, the CMRR and common mode gain of the opamp, so let us directly write down the expression for the CMRR of the opamp. As we know the CMRR of the opamp purely depends on the g_m of the input device and the output resistance of the current source transistor. So, to do that, so this is nothing but $1 + 2 g_m R_{out}$, where R_{out} is the output resistance of the current source, so that is $1 + 2 g_m (R_{D1} || R_{D2})$ and $R_{D1} || R_{D2}$ is $1 / (\lambda_n I_{D1} || \lambda_p I_{D2})$. Which is simply $1 / (0.02 \text{ times } I_{D1} || I_{D2})$, which is as we can see from the original opamp, it is 1 million. And therefore, the output resistance of M_0 is 50 kilo ohms, this means that the CMRR of the opamp is equal to $1 + 2 \text{ times } 2 \text{ millisiemen times } 50 \text{ kilo ohms}$ and this is 201.

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* Noise of M_0 :

@ XY: i_{dn0} splits into 3 paths

source of $M_1 \Rightarrow Y_{gm1}$
 " " $M_2 \Rightarrow Y_{gm2} = Y_{gm1}$
 drain of $M_0 \Rightarrow Y_{ds0} \gg Y_{gm1}$

100kΩ 500Ω

KCL @ output node
 $i_{scn} = 0$
 \Rightarrow Noise from M_0 does not appear @ output
 (does not appear in input-referred noise)

Last but not least, we need to look at what happens to the noise of M_0 because that has not been covered so far. So, let us briefly look at that. So, this is the noise of the current

source transistor. So, in this particular case, let us assume that the output is short circuited to ground, so that you are trying to find out the short circuit current. Now, if the transistor M_0 has a current i_{dn0} , this current source now enters the node x_y and at x_y i_{dn0} splits into three parts. So, the three parts are there is current flowing into the source of M_1 , there is current flowing into source of M_2 , and there is current flowing into drain of M_0 .

The impedance looking up at the source of M_1 is approximately $1/g_{m1}$ which is a very low impedance node. The impedance looking up at the source of M_2 presents an identical impedance $1/g_{m2}$ which is equal to $1/g_{m1}$. And finally, looking down to the drain of M_0 , it sees an impedance r_{d0} , which is much much larger than $1/g_{m1}$. As you can see r_{d0} is 100 kilo ohms, and $1/g_{m1}$ is approximately is 500 ohms. So, as you can see all of the current flows up into the sources of M_1 and M_2 , and half of the current flows through M_1 and half of the current flows through M_2 . So, this current splits equally between these two paths these two currents are correlated. So, you cannot use i_{dn0}^2 you have to calculate the total current while using the linear quantities. So, there is a current $i_{dn0}/2$ flowing through M_1 and the same amount flowing through M_2 .

Let us see what happens to the current flowing through M_1 that current flows through M_3 to create a small signal noise voltage which I will call V_{xn} and that noise voltage causes a noise current to flow through M_4 . Now, clearly, since M_3 and M_4 are identical, this noise is also $i_{dn0}/2$, which is the same as this noise.

Now, let us look at the total output short circuit noise current if you apply KCL at the output node you find that I_{scin} is equal to 0, because the current entering the node from M_4 is exactly equal to the current entering leaving the node into M_2 . Therefore, there is no current flowing into the short circuit. This means that the noise from M_0 does not appear at the output. So, this is a very important result; and consequently it also does not appear in the input referred noise of the opamp. So, as you can see the noise of M_0 appears through the transistors M_1 and M_2 , but does not affect the output at all.