**Analog Integrated Circuits**
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**Lecture – 21**
**One-Stage OpAmp Slew Rate**

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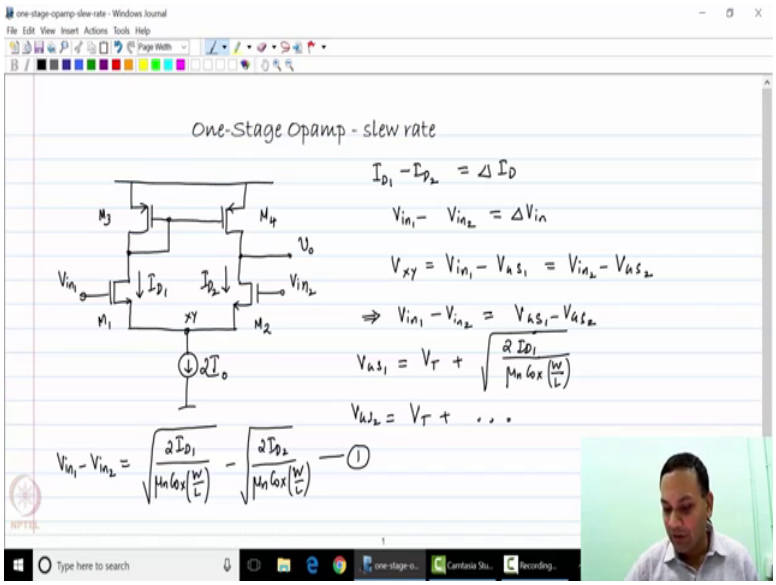


In this lecture, we are going to study a specific property of the opamp called slew rate. Before we study that we actually need to understand a particular characteristic of the opamp namely what are called the large signal transfer characteristics. So, what I am interested in is calculating I D 1 minus I D 2. So, in other words, this is the differential current flowing through M 1 and M 2. I want to find this as a function of the differential input voltage which is applied and I am so which is V in 1 minus V in 2 that is delta V in. So, in other words, I want to plot I D 1 minus I D 2 as a function of V in 1 minus V in 2.

Now to do that I need to first calculate analytically I D 1 and I D 2 or the difference as a function of the input voltages. So, to do that, I need to write down the correct equations of the opamp of the transistors. So, first of all, let us assume that the total current through the opamp is 2 I naught, so that each of M 1 and M 2 has a current I naught. So, before we write it in this manner. So, we can write the voltage at node x y as V in 1 minus V GS 1 or V in 2 minus V GS 2. So, clearly these two quantities have to be equal. This means that V in 1 minus V in 2 has to be equal to V GS 1 minus V GS 2.

Now, what do we know about V GS 1, V GS 1 is nothing but V T of the transistor plus root of 2 I D 1 over mu n c ox W over L. And similarly, V GS 2 is V T plus root of two I D 2 over mu n C ox W over L. So, therefore, V in 1 minus V in 2 is equal to root of 2 I D 1 over mu n C ox W over L minus root of 2 I D 2 over mu n C ox W over L. This is the first relation I will denote this as equation one, this is the first relation between I D 1, I D 2 and V in 1 V in 2. Remember that V in 1 and V in 2 are the known variables, and I D 1 and I D 2 are the unknown variables for this particular calculation.

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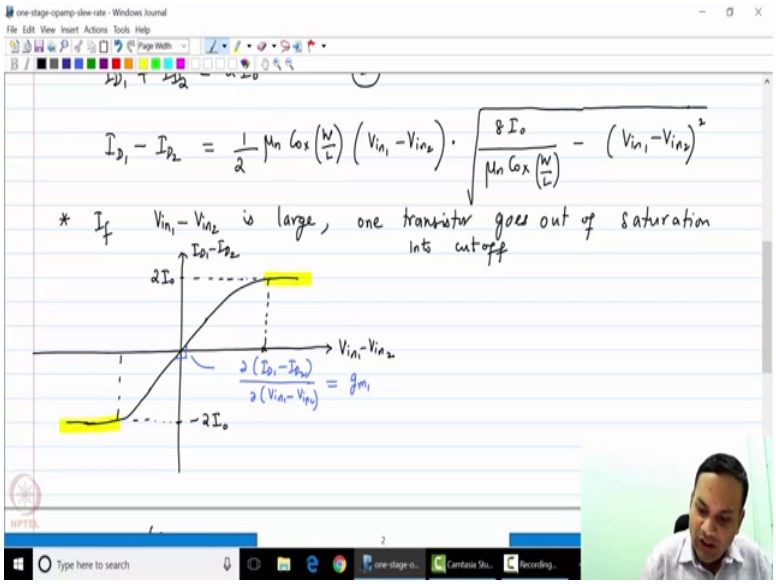


The second relationship is simply KCL at node x y which tells us that I D 1 plus I D 2 always has to be equal to 2 I naught. So, I will denote this by equation 2. Clearly, I have two equations and two unknowns, so I should be able to solve for I D 1 and I D 2, but more specifically I am interested in solving for I D 1 minus I. It turns out that if you solve these equations for I D 1 minus I D 2 you will get the following relationship. So, you can of course, do some arithmetic manipulation. So, it turns out that I D 1 minus I D 2 depends on V in 1 minus V in 2 in the following manner. So, I D 1 minus I D 2 is half mu n C ox W over L into V in 1 minus V in 2 times square root of 8 I naught over mu n C ox W over L minus V in 1 minus V in 2 the whole square. So, clearly I D 1 minus I D 2 is an odd function of V in 1 minus V in 2. Now, what happens when V in 1 minus V in 2 is 0, if that happens clearly I D 1 should be equal to I D 2 which means they are both equal to I naught. So, this equation is clear on that.

Now, if V in 1 minus V in 2 becomes large enough it turns out that this equation is no longer valid because we have assumed in calculate writing down this equations, we have assumed that both transistors are in saturation. If V in 1 minus V in 2 is large, one of the current starts decreasing, the other current starts increasing because clearly I D 1 minus I D 2 is finite. So, one goes out of saturation. So, this is something to keep in mind. So, if you were to plot I D 1 minus I D 2 as a function of V in 1 minus V in 2, it turns out that for very small V in 1 minus V in 2 this particular relationship is linear, because you can assume that you can linearize this particular expression to get a linear dependence. If V in 1 minus V in 2 becomes large, it turns out that this particular relationship becomes non-linear in some manner that you can determine by plotting this curve.

Now, what we are interested in are a couple of points on this curve. So, first of all, we are interested in finding out what value these two points are. So, clearly when this happens you can see that I D 1 minus I D 2 becomes a fixed value, and that happens when one of the transistor goes out of saturation into cut off. When that happens let us say M 2 turns off then all of the current flows through M 1; in other words this total current has to be equal to 2 I naught. On the other side, if V in 1 minus V in 2 becomes very goes negative and large the all that the current flows through M 2, and therefore, I D 1 minus I D 2 is minus 2 I naught because I D 1 becomes 0, and I D 2 becomes minus 2 I naught.

Now, another property of this is that the slope around the origin has to be equal to the derivative of I D 1 minus I D 2 over dope V in 1 minus V in 2. And from small signal analysis, we know that this is equal to g m of the differential pair and that is why it happens to be linear around the origin. Now, of course, once it reaches this point, the transistor no longer has any transconductance.

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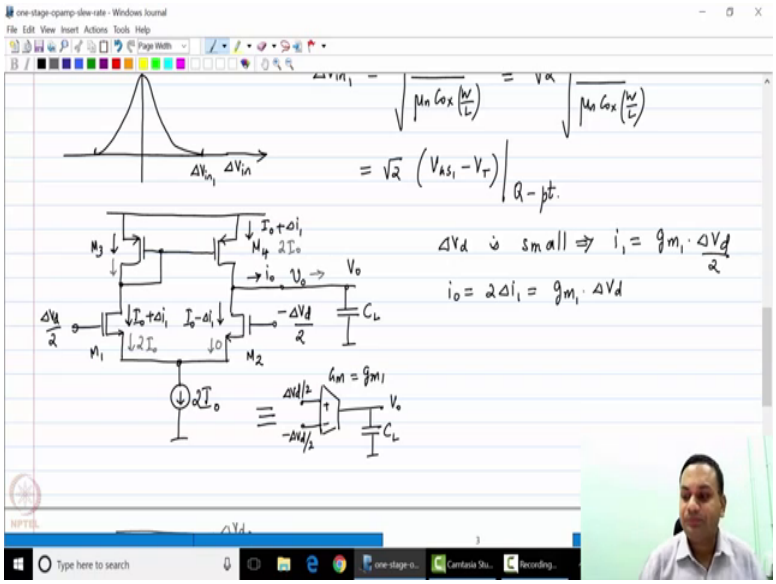

For example, if you were to plot the transconductance of the device, the transconductance of the differential pair as a function of delta V in, it would look something like this; it would go to zero at some point. Our job is to find out at what point this full switching happens. In other words, I am trying to find out at what voltage the current fully switches from one side to the or fully switch to one side. It turns out that happens when the gate source voltage of one transistor falls just exactly to its threshold voltage; and that can easily be calculated now as delta V in, I will call that delta V in 1. This delta V in 1 happens to be equal to root of 4 I naught over mu n C ox W over L.

Now, I am going to rewrite this in a specific manner, I am going to rewrite this as root of root 2 into root of 2 I naught over mu n C ox W over L. And you can clearly see that this is nothing but root 2 times V GS 1 minus V T at the quiescent point. So, if you were to take the quiescent point of the differential path, and calculate the V GS 1 minus V T which is the overdrive voltage or the V D sat of the device. And if you were to apply root two times that voltage at the input of the differential path all of the current would switch to one side and that is this point delta V in 1.

Now, we are interested in this for a very specific reason, we are now going to study what will happen if you start applying incremental steps to the input of the opamp. So, I am going to take the opamp, and I am going to start applying incremental voltage steps, so delta V d by 2 and minus delta V d by 2. So, in other words, I am applying an

incremental voltage differential voltage of delta V d at its input. And let us say that the opamp is driving some load capacitance C L as we have seen before the opamp or a normally drives a capacitive load because transistors present a capacitive load when seen from the gate. Let us say this output voltage is V naught.

Now, if I were to apply a differential voltage delta V d, let us first start by assuming delta V d is small. If delta V d were small, I can calculate what i o is. I am now going to write down the total currents through the transistor this current is I naught plus some sorry I naught plus some delta i 1 this current is I naught minus delta i 1 where delta i 1 is equal to g m 1 times delta V d by 2. Of course, what is going to happen is that this current is going to flow through M 3 and get mirrored down to M 4. So, current through M 4 is I naught plus delta i 1 and so the incremental current total incremental current of 2 delta i 1 flows through the capacitance C L. So, I naught is 2 delta i 1 which is clearly g m 1 times delta V d.

So, clearly the one-stage opamp acts like a transconductance of value g m. If I were to replace it with a block diagram, it would look like this; it would look like a transconductor whose value is small g m 1. So, this is delta V d by 2 minus delta V d by 2, this is what the model of the opamp would look like.

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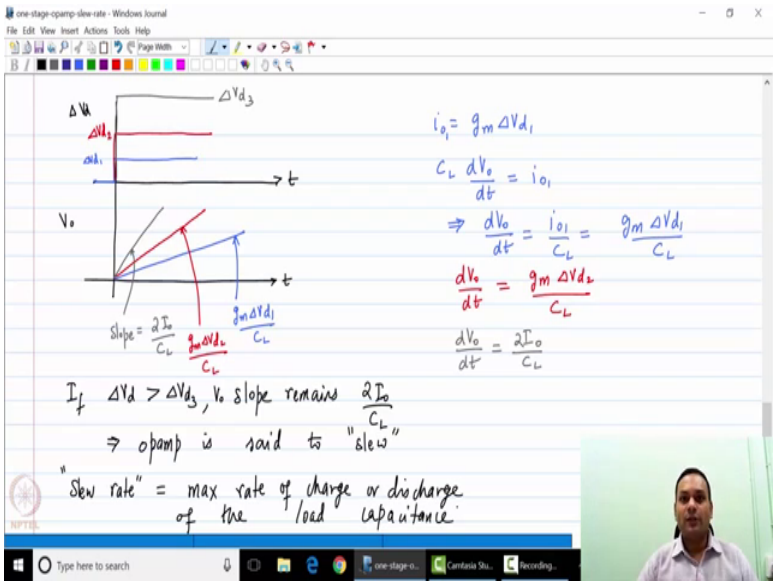


So, if I were to plot the input and output voltages. So, let me first plot the input voltage. I am giving a small step voltage in the input. The output voltage now, remember the x-axis

is time; and here this is delta V d, and this is V o. So, for this particular delta v d let me call that delta V d 1. So, i o is equal to g m times delta V d 1. So, this i o 1 and for the capacitance I can say C L d V o by dt is equal to i o 1 because all of this current flows through the capacitor and therefore, d V o by dt is i o 1 by C L which is g m delta V d 1 by C L. Clearly, the d V o by dt is a constant because delta V d 1 is constant C L is constant and g m is constant, therefore, the output rises as a ramp because the output current is constant.

Now, let us say I increase the value of delta V d 1 to delta V d 2, I apply a larger step at the input. In that case, d V o by dt is equal to g m delta V d 2 by C L and so on. So, it would rise with a as a faster ramp. Now, if I were to apply a large enough step if I were to apply large and a larger step. Let us assume I apply a very large step delta V d 3, what would happen is that the largest current that can flow out of the device is clearly limited because at that point what would happen is all of the current 2 I naught would flow through M 1. So, this current is 2 I naught, this current is 0; and this 2 I naught current flows through M 3 and flows out of M 4 into the output.

Now, please note in this case d V naught by dt no longer depends on delta V d, it is simply 2 I naught over C L. So, this ramp would rise at the rate of 2 I naught over C L. Now, the important thing to note is that the important thing to note is that if you were to increase the slope any, if you at increase delta v d any further you would not get any further increase in the slope of the output voltage that is important to remember. So, I will just write down the slope numbers here, this slope is g m delta V d 1 by C L and this is g m delta V d 2 by C L. So, it is important to remember if delta V d is larger than delta V d 3 slope V o slope remains as 2 I naught over C L, you cannot charge the capacitance any faster. In such a case, so the opamp is said to slew and the maximum rate at which the opamp can charge or discharge a load capacitance is called as slew rate. So, the slew rate is the maximum rate of charging charge or discharge of the load capacitance.

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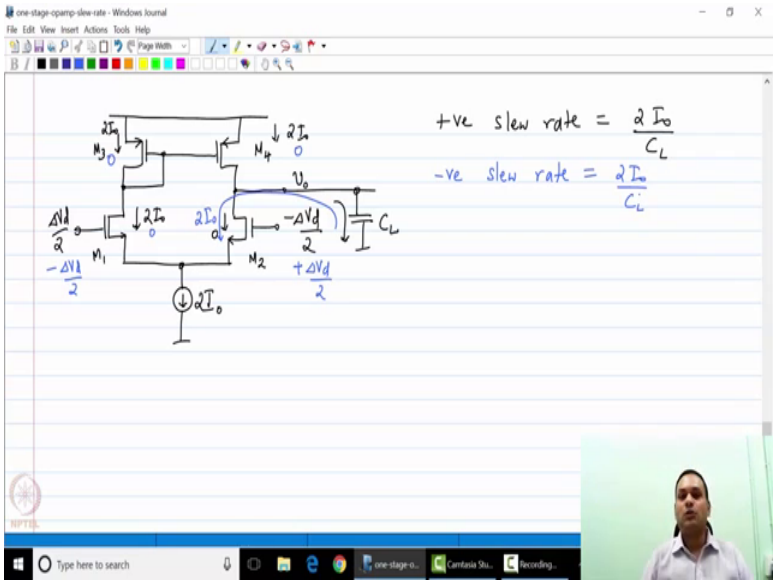


So, let us now find out what the slew rate of the opamp is. So, let us take this opamp and let us apply a positive step. And let us assume that the opamp is charging some load capacitance C L. As we have seen in this particular condition, the M 1 assuming that this is a positive step M 1 carries all of the two current 2 I naught M 2 has 0 current, this current is 2 I naught, M 4 carries 2 I naught and that is the rate at which the capacitance is charged. So, the positive slew rate is said to be 2 I naught over C L.

Now, what happens if a negative step is applied, let us say you were to apply minus delta V d by 2 to M 1 and plus delta V d by 2 to M 2. If that were the case, M 2 would have a current 2 I naught, and M 1 would have 0 current, M 3 would have 0 current, M 4 would have zero current. So, M 1, M 3 and M 4 would be cut off and all of this current all of this current would be pulled out of the capacitor C L, so that C L would discharge at a maximum rate of 2 I naught over C L. And this also happens to be the negative slew rate.