Analog Integrated Circuits
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Lecture – 20
One-Stage OpAmp Noise & Offset

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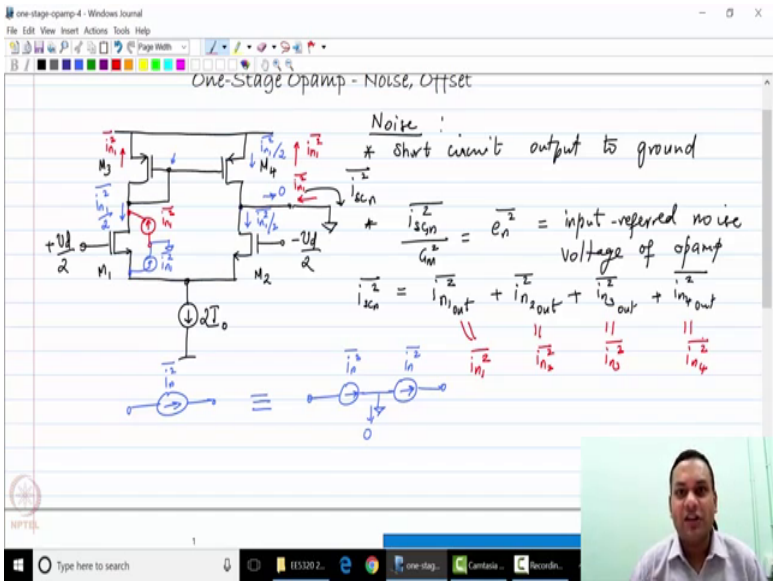

In today's lecture, we are going to look at the noise and offset of the one-stage opamp. So, let us first draw the circuit of the one-stage opamp that we have been looking at. So, for this particular analysis, I am going to assume that the current source at the bottom is ideal. So, at the end, we will see what happens if the current source also produces noise of its own. So, the current source has some current 2 I naught; and I am going to number the transistors input transistors M 1 and M 2; and these transistors the PMOS load transistors are M 3 and M 4.

Now, the way I am going to approach this is I am going to calculate the noise, I am going to short circuit the output. So, I am going to short circuit the output to ground. And I am going to calculate the short circuit noise current. So, I am going to call that i scn square. Then I am going to divide the short circuit noise current over the transconductance of the opamp, which I will denote by capital G m. And if I divide this by the square of the G m of the device I will get the input referred noise voltage squared which I will denote by e n square, this is the input referred noise voltage of the opamp. This is the same procedure

we have used even for simpler circuits. This is very useful because opamps in general are voltage control current sources, the CMOS opamps that we are looking at.

So, now, let us consider each noise source in turn, I have four noises. Let us assume that each transistor produces a noise which we will denote with the subscript 1, 2, 3, 4. So, I am going to say that the total noise is the sum of the individual noise currents at the output i n 1 squared out i n 2 squared out plus i n 3 squared out plus i n 4 squared out where each of these terms is the contribution of the corresponding transistor. And we will take one or two of these, and then we will generalize to the actual output noise current.

So, let us just take the noise of n 1 alone. So, let us say this is the noise of n 1. Now, the way I am going to do this is I am going to as we know the way we have approached this for noise is we have said that this is the same as having two current sources in series as far as the nodes of interest in the network are concerned, it does not change. And moreover, you can also ground the central node, there is no current through the central node, and therefore, there is no problem in connecting that to ground, this is exactly the strategy that we are going to adopt.

So, I am going to take this, and I am going to split these into two current sources, I am going to use two different colors. So, for the top one, I am going to use red; and for the bottom one, I am going to use blue. And this center point is grounded. And so both of these are equal to i n 1 squared. Now, again the corresponding currents in the circuit I am going to replace by the corresponding colors.

So, let us simply look at the blue colored values alone. So, I have a current i n 1 squared which is flowing out of this node. And at this point, this current source i n 1 squared sees two transistors M 1 and M 2. On both sides the input impedance is 1 over g m and because you are looking into the source of the transistor, and therefore, there is going to be a current, there is going to be a current through M 1 of value i n 1 squared over 2. And there is going to be a current through M 2 of value i n 1 squared over 2.

Now, what happens to this current on the left side, the current through M 1 will flow through M 3 to create a small signal voltage here. And that small signal voltage will also force a current through M 4 equal to i n 1 squared over 2. And if you apply KCL at this node, so now, let me change this color. So, that there is no confusion I will change that to black, so that there is no confusion. So, as you can see if you apply KCL at this node for

this blue colored currents the noise current flowing through this side is 0, because M 4 is pushing i n 1 squared over 2, and M 2 is absorbing i n 1 squared over 2. So, there is no noise current flowing due to the blue current source.

What happens to the red current source i n 1 squared? So, let us now look at that. So, if I look at this current, now this current is flowing into this node, and it turns out that this current is actually going to try to split between M 1 and M 3. Now, as you can see M 1 presents an impedance looking down at its drain of r d s, whereas M 3 presents an impedance which is 1 over g m 3. And clearly 1 over g m 3 is going to be a much lower impedance and therefore, this current is going to flow most of the current is going to flow through this transistor.

If that happens then that current will automatically get mirrored into M 4 also. There is no noise current through M 2; and all of this current will flow into the short circuit at the output mode. The direction of the current does not matter because this is a noise current, you are only looking at the square of the noise current, it is only the noise power that matters, so clearly all of noise of M 1 ends up at the output node. What about M 2 as you can imagine, you will see the same effect for M 2 also, you can analyze it and show that all of the noise of M 2 also turns up at the output. Now, let us quickly see what will happen for noise of M 3. So, to do that, I will create a copy of this on the next page, so that we can analyze this separately.

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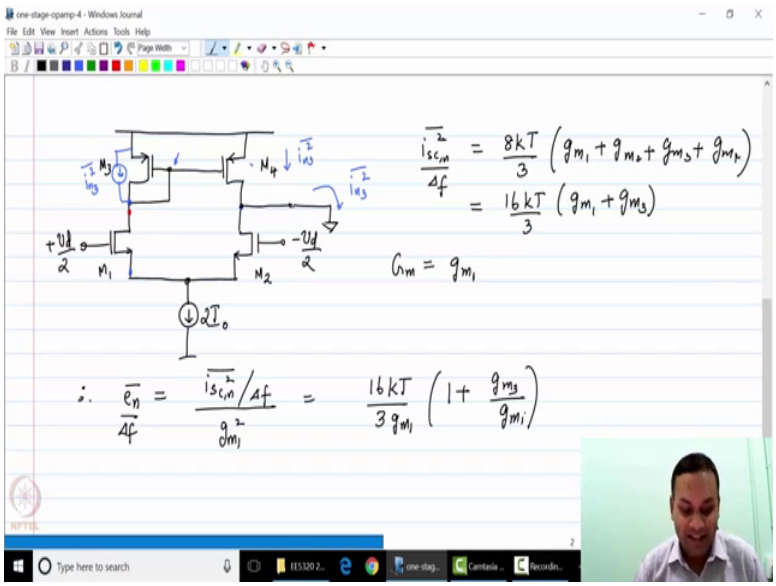

So, now let us assume that M 3 has some noise current, which is i n squared 3. Now, what happens to this current, clearly the V DD node is a small signal ground for noise analysis. Now, at this node the current i n 3 tries to split in two directions. And you can clearly see this is very similar to the red color noise source that we just analyzed on the previous page. And you can see that all of this current would try to flow back into M 3 itself, it would generate a small signal noise voltage here; and it would cause a current i n 3 squared to flow here, and it will flow through the output. So, there will be a current i n 3 squared flowing into the output. And you can apply a same analogy for M 4 also.

Therefore, you can clearly see that this is i n 3 squared and this is i n 4 squared. So, it turns out for this one-stage opamp all of this current, M 1 all of the noise currents of M 1 M 2, M 3 and M 4 will flow through the output. Therefore, the total short circuit noise current of the transistor is nothing but 8 K T by 3 into g m 1 plus g m 2 plus g m 3 plus g m 4. And if into delta f and now if I am looking at the density - power density spectral density, then this is 8 K T by 3 into the sum of all the g ms. Now, this can be further simplified, because the two paths are identical I can now write it as 16 k t by 3 into g m 1 plus g m 3. So, this is the short circuit noise produced by the one-stage opamp.

Now, what is the overall trans-conductance of the opamp. So, this is nothing but the short circuit current over the input applied voltage V d that is clearly just g m 1 of the input transistors, therefore the input referred noise voltage of the transistors is nothing but the short circuit noise current density squared noise squared density over g m 1 squared. So, this is nothing but 16 K T by 3 g m 1 into 1 plus g m 3 by g m 1. Now, the important thing for us is to understand how to reduce noise because that is going to be critical to maintain the SNR of the signal.

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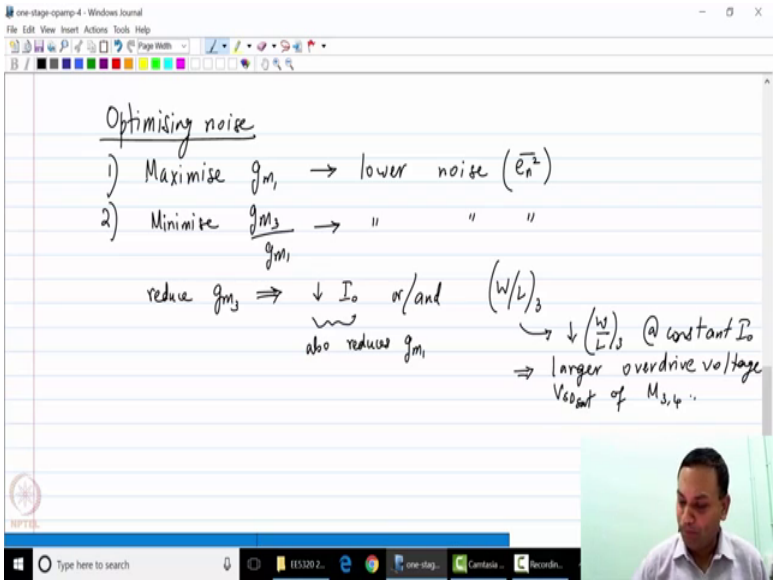

Now, as far as optimizing noise is concerned, so the first thing you need to minimize is or first thing you need to do clearly larger the value of g m 1 lower will be the noise. It is clear that the input referred noise voltage squared e n squared is nothing but is inversely proportional to it decreases as g m 1 is increased. It is not just inversely proportional there is some you know squared term also, but it is clear that as g m 1 increases the value of e n squared will go down. Now, the other thing you know is to minimize g m 3 over g m 1. So, clearly if you reduce the relative trans-conductance of M 3 and M 4 relative to M 1 and M 2, you will also reduce noise that is also cleared from the second term in the noise.

Now, how do you reduce g m 3, it turns out that to reduce g m 3, you need to reduce either I naught or the width to length ratio of 3 and 4, I naught is of course, the bias current of 3 and 4. Now this term also affects g m 1 and many other parameters of the opamp, so you would not prefer to do this. And therefore, the only option is to reduce g m 3. So, if you decrease is the only option is to reduce the width to length ratio of 3. Now, if you keep the current constant and reduce the width over length, it turns out that the overdrive voltage of the PMOS transistors will start increasing. So, in this particular design, you want to maximize the overdrive voltage of M 3 and M 4 that would give you best noise performance.

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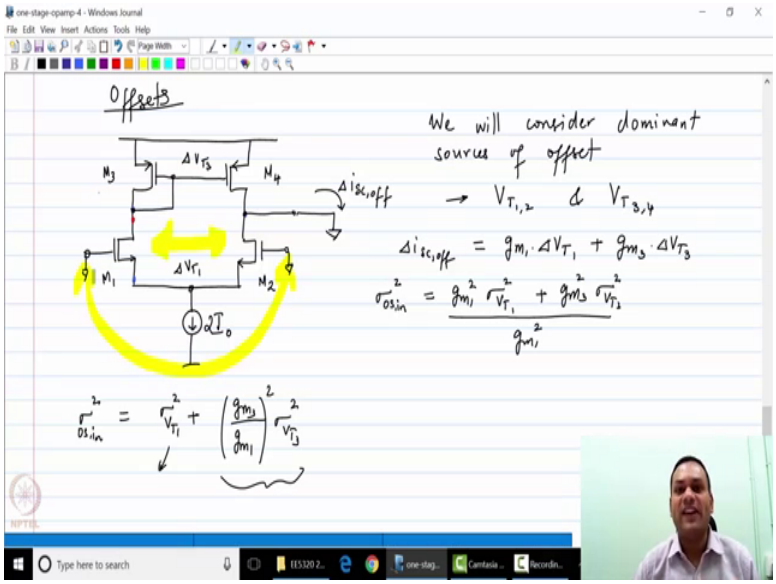

Now, what about offsets, it turns out that you can use the same technique you can use the same type of analysis to analyze offset also. And what we are going to do is we are going to simplify our analysis of offset. We are going to follow the exact same procedure; we are going to assume some mismatch. And we are going to look at the offset current short circuit offset current flowing through the output. So, we are interested in offset current flowing through the output. And we will apply mismatch to different portions of the circuit, and calculate the offset current we will divide it by the trans-conductance squared to get the sigma squared of the offset at the input.

So, now the dominant sources will be considered. So, these are V T of 1 and 2, the threshold voltage mismatch between 1 and 2, and the threshold voltage mismatch between 3 and 4, these are the two dominant sources of offset in the circuit and this is what we are going to consider for this particular analysis. So, let us assume that the there is a delta V T 3 mismatch between 3 and 4, and there is a delta V T 1 mismatch between transistors 1 and 2. In other words, transistor M 1 may have a voltage of threshold voltage of delta v of V T 1 M 2 will have a threshold voltage of V T 1 plus delta V T 1.

So, if you do this you can clearly show that if you short if you connect the inputs to ground, you will see that if the threshold voltages are not equal, there will be an offset current flowing through the short circuit and it turns out that the and let us call that delta i sc off. And this value of offset current is clearly going to be g m 1 times delta V T 1

plus g m 3 times delta V T 3. That is purely because the a difference in offset voltage between M 1 and M 2 can the offset voltage delta V T 1 can be considered as small increment on top of the bias point and same thing with M 3 and M 4. And therefore, you can write the difference in the currents between M 1, M 2 as g m 1 times delta V T 1, the difference in currents between M 3 and M 4 is g m 3 times delta V T 3. And clearly both of these the sum of these two will flow through the output short circuit.

Now, therefore, you can now write the sigma squared, the sigma squared offset at the input is clearly g m 1 squared sigma squared V T squared V T 1 squared plus g m 3 squared sigma squared V T 3 squared over the trans-conductance squared which is g m 1 squared. Therefore, the input referred offset sigma squared is nothing but sigma squared V T 1 squared plus g m 3 over g m 1 squared times sigma squared V T 3 squared. Now, if you want to minimize the input referred offset, we again know what to do we need to maximize g m 3 sorry we need to minimize g m 3 and maximize g m 1, so that this term goes to 0. Now, you can see this term becomes negligible. You can see that the offset voltage of the input pair appears directly as an input referred offset voltage that is very important to note. The offset of the input pair M 1 and M 2 appears directly at the at the input as an input referred offset there is not much you can do about it except to reduce sigma squared V T 1 squared itself.