Analog Integrated Circuits
Prof. S. Aniruddhan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 02
Simple MOSFET Circuits

In the previous class, we solved the basic small signal model and the current voltage relationships for the drain current versus the gate source and drain source voltage of the MOSFET. In today's class, we look at some simple MOSFET circuits and see what the small signal behavior of those circuits us.

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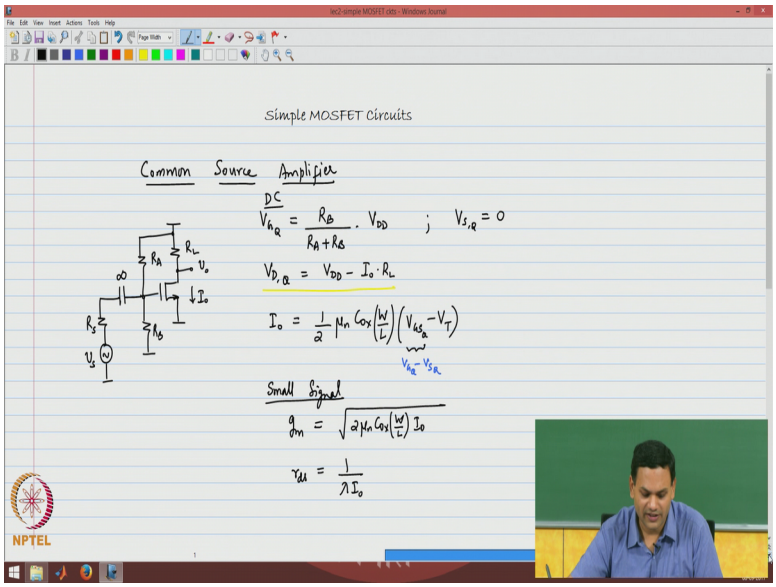

So, let us start of the first circuit that will look at is the common source amplifier. So, I will draw one version as with circuits in general. There are many different versions of the common source amplifier, I will draw the simplest possible version where the source terminal is common to the input and output puts and the drain terminal is where the output is taken and the gate terminal is the input port, where the input signal is applied.

Now, at the gate port the DC and AC signals are separated using a very large capacitor; I will show it is an infinite capacitor, but is usually a very large capacitor. And before we draw the small signal, let us do the DC circuit analysis first. The capacitor is an open circuit and therefore the voltage at the gate which I will represent as V G Q, representing the quiescent gate voltage is nothing, but R B by R A plus R B times VDD. As you can

see in this version of the circuit, we are generating the gate voltage from the supply voltage itself; the quiescent source voltage of course is 0. Because in this case, we have grounded the source voltage and the quiescent drain voltage is V D B minus; I naught times R l, where I naught is the bias current through the MOSFET.

Now, what is this bias current? So, that is an additional DC parameter for the circuit I naught is related to the gate source voltage in the following manner. Please note that normally to calculate the operating point for hand analysis; we do not consider the R D S of the MOSFET. So, we do not consider any dependence on the drain source voltage and by writing this equation.

We have also assumed that the transistor is properly biased in the saturation region and of course, V G S Q is nothing, but V G quiescent minus V S quiescent. So, once VDD is known and R A and R B are known, you can find out the quiescent gate voltage. In this case that also happens to be the quiescent gate source voltage and the drain current is known and therefore, the drain quiescent voltage is also known, so we are done with the DC.

The next step is to calculate the small signal parameters of the circuit. So, the small signal parameter of interest; so, this is DC for small signal analysis. The first step is to calculate the small signal parameters of interest; in this case there are two parameters as we saw last class. The first one is the g m or the transconductance of the MOSFET, so this is a function of the device parameters mu n c ox W over L and the bias current I naught and R D S is a function of lambda and we saw last class that it is equal to 1 over lambda I D; if you know lambda right and the bias current you can find out the R D S of the transistor.

Now, once you know the small signal parameters the next step is to build the small signal equivalent circuit for this amplifier.

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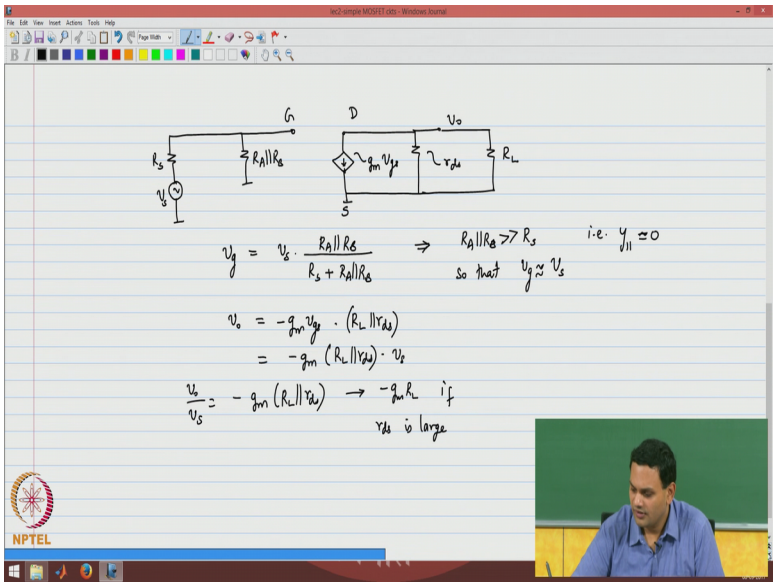

So, the capacitor happens to be a short circuit because it is an infinite capacitor VDD is signal ground. And therefore, the two resistors appear in parallel R A and R B appear in parallel at the gate of the device at the drain is where you take the small signal output voltage and you have two parameters one is R D S the other is g m times V G S, which is the voltage control current source and apart from this you also have the load resistance R L.

So, systematically the gate voltage is the small signal gate voltage is nothing but the input voltage V S modified by the resistive divider formed by R S R A and R B. Now as we know from our basic circuits knowledge this means that we want R A parallel R B to be much much larger than R S. So, that the gate voltage is approximately equal to the input signal voltage V S and this also means that the amplifier as a two port will have a y 11 which is almost 0; which is a precondition for large amplification large k.

The next step now is to write the voltage at the output the voltage at the output is nothing, but g m V G S times R L parallel R D S and with the negative sign of course, because the current is being pulled out of the node for a positive source voltage and this is nothing, but minus g m into R L parallel R D S times V S assuming that V g is approximately equal to V S. Therefore, the gain of the amplifier V o by V S is minus g m into R L parallel R D S, if the circuit is designed such that R D S is very large then they gain would tend towards minus g m; R L let us look at a slightly different circuit.

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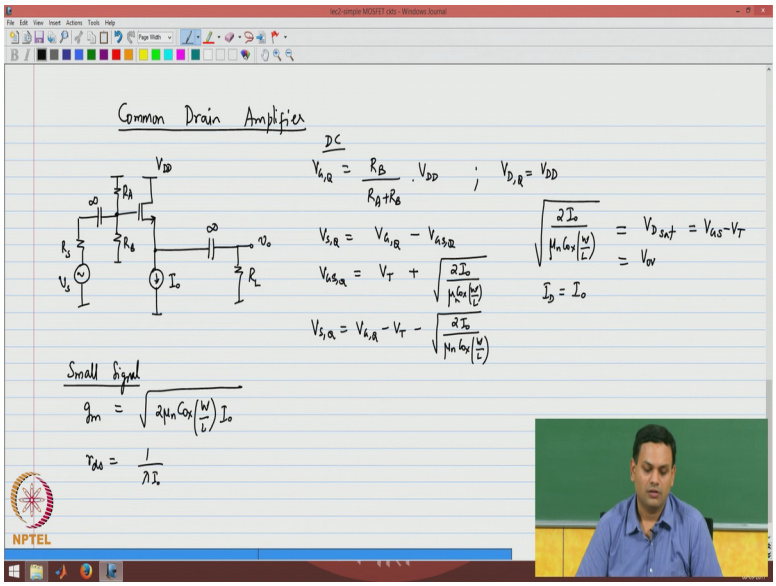

The next circuit that we are going to look at is the common drain amplifier since we want to move on to analogue ICS. So, we will look at just these two structures for amplifiers and then look at some biasing circuits also.

So, if you look at the common drain amplifier in now instead of the source terminal; it is the drain terminal that is common to both input and output ports and the gate voltage is biased at a constant voltage again using a resistive divider. At the source terminal, you have a current source that sets the bias current through the transistor. And since you do not want a typic; very often you do not want DC current through the load, you have an infinite capacitor at the output side also and the output is taken across the load resistance R L.

Now, again we can go through the same procedure; we will write down the DC parameters for the circuit, the DC voltages and currents. Then we will figure out the small signal parameters from the DC voltages and currents. And then we will figure out the gain of the circuit, now the quiescent gate voltage is again R B by R A plus R B times VDD; that happens to be the same as before. But this circuit is slightly different in the case; in the sense that it is now the drain voltage that is constant and it is equal to VDD and the source voltage is figured out by subtracting the gate source voltage from the gate quiescent voltage.

So, then the next question is what is this gate source quiescent voltage? This is now a function of the bias current through the transistor which has to be equal to I naught and therefore, this gate source voltage can be written as V T plus root of I naught over mu n c ox W over l. I have derived this last equation purely from the device current voltage characteristics. And therefore, the quiescent voltage is this expression. Now, one last thing to note as an aside this parameter; root of two I naught over mu n c ox W over L is often called the V D; sat of the transistor or V D S sat of the transistor.

This is nothing, but V G S minus V T at the operating point at the quiescent point. So, this is a very very useful parameter for the circuit, as we will see going forward this is also often called the overdrive voltage. Because it is the voltage over and above the threshold voltage required for the device to conduct a particular value of DC current. So, it has many different names, so we have figured out the voltages finally. Of course, the drain current is nothing but I naught because in this particular case unlike the last common source amplifier, we have biased at using a current source.

Now, let us move on to this small signal analysis this was DC so far. So, again the first step is to figure out the g m and since we know the current again figure out the g m and as before R D S is 1 over lambda I naught.

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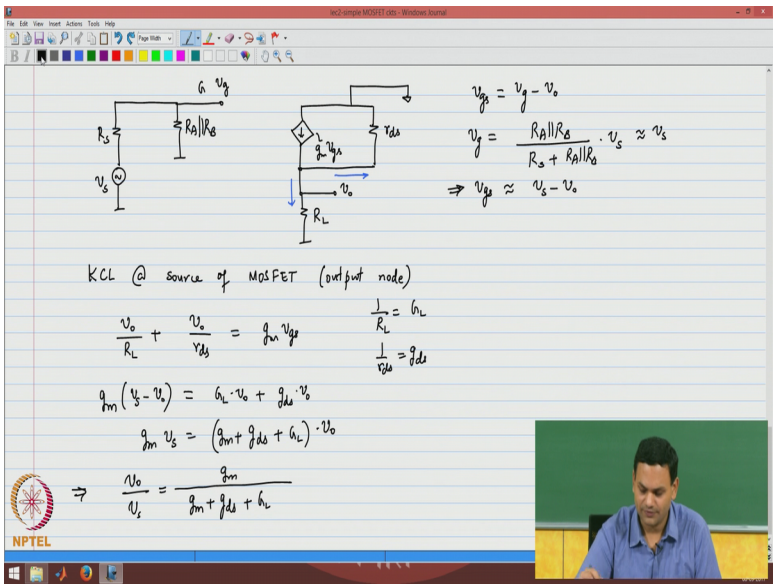

So, now we can draw the small signal equivalent circuit at the gate terminal; the small signal equivalent circuit look similar, on the output side there is some small difference as

we will see this is g m times V G S and this is R D S. But now it is the drain terminal is at small signal ground and at this point the current source is an open circuit for small signal and you have the load resistance R L.

Now, we will point out that V G S for the transistor is V G minus V o. So, now we need to figure out what V g is V g is R A parallel R B by R S plus R A parallel R B times; V S. And as we know, normally we want all of the voltage input voltage source to appear at the gate and we will say this is approximately equal to V S. And we know that will happen when the R A parallel R B is chosen to be much larger than R S, in this case V G S is approximately equal to V S minus V naught.

Now, we will apply k c L at the source node of the MOSFET which also happens to be the output node. So, the current flowing out of the node is V o by R L plus V o by R D s. So, those are the currents flowing in this direction and this direction and this should be equal to the total current flowing into the node which happens to be g m V G S. So now, to make things simpler; I am going to write it in terms of the conductances note that 1 over R L is G L and 1 over R D S is G D S, you can write the equation in terms of the conductances; sometimes it makes things easier to visualize.

So, now g m times V S minus V o is equal to G L times V o plus G D S times V o and therefore, g m times V S is g m plus G D S plus G L times V o and this gives us the expression for the gain of the device gain of the amplifier. This is the ratio of g m to the sum of g m plus g D S plus G L. So, this is the common drain amplifier gain as you can see the gain of the common drain amplifier is positive. Whereas, the gain of the common source amplifier was negative I think that is something you should remember.

Please note the negative sign here and in the case of the common drain amplifier, the gain is positive.

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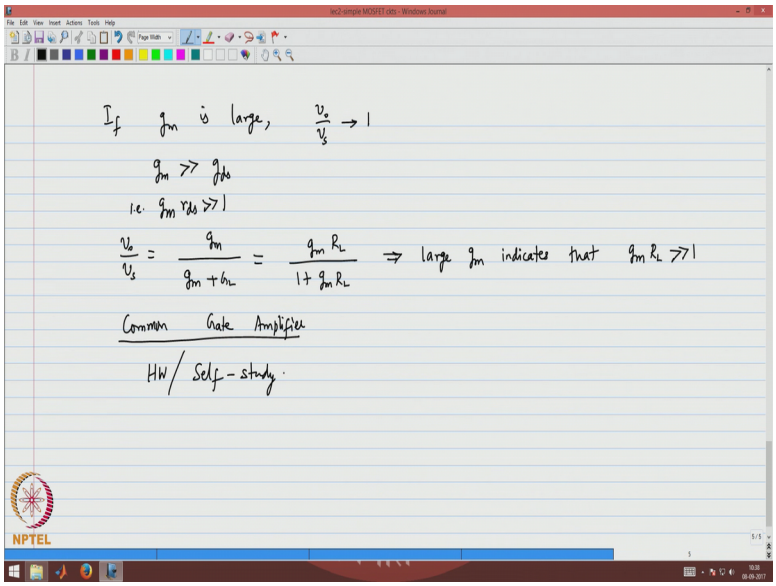

What else can we understand from this if g m were large then the gain of this amplifier tends to 1. So, let us see what we mean when we say g m is very large, so to do that will make one approximation we will say that normally for a device g d s can be chosen such that g m s much much larger than g d s. In other words, what I am saying is the intrinsic gain of the device g m; r d s is usually much greater than 1; this is of the order of several tends or maybe even close to 100 and therefore, g d s can be neglected with respect to g m.

So, now I will write the gain like this but now I can substitute for G L to be 1 by R L and now this tells you what g m means. So, when we say large g m if you want to be more specific g m should be chosen to be large enough such that g m; R L is much much larger than 1.

So, for a particular load resistance g m should be chosen large enough such that g m; R L is much larger than 1; also please note that the gain of the circuit is normally never greater than 1. Similarly, there is a third circuit called the common gate amplifier the I will leave the analysis of this circuit as an exercise for the viewer.

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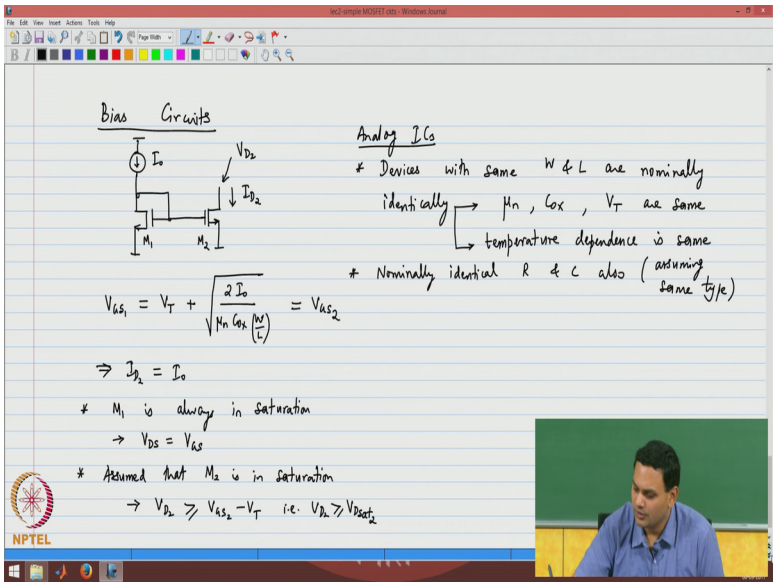

Next, before going forward let us look at some simple bias circuits using MOSFET's; you may remember from your basic circuits course that it is possible to generate; use a current source to generate the required gate source voltage. For a MOSFET, I am going to name these; now that we have multiple MOSFET's, I am going to call them M 1 and M 2.

So, now one of the things will rely upon as you will see this becomes more and more important as we go ahead in the course. So, in analogue ICs we will assume certain things on the same IC devices with same width and length are nominally identical. This is not true for discrete devices, if I go to the market and they get it by a discrete MOSFET; if I buy two of them; I am not assured that they have identical behaviors. Whereas, if I choose, if I designed two MOSFET's on the same integrated circuit, I am assured that they are nominally identical as long as they have the same dimensions. What does this mean? This means the behavior of these devices of two such devices is identical with respect to the device parameters. So, they will nominally have the same mobility, same oxide capacitance and same threshold voltage.

The other thing you can say is that the minute their on an IC, they are very close to each other and therefore, they will experience very similar temperature changes and therefore, you can assume that the temperature dependence is also the same. In other words, if the temperature changes; let us say the temperature increases normally, the mobility of the

holes or electrons falls with increase in temperature; in such a case you can assume that if you have two devices on the same IC; their mobilities will change by the same percentage amount.

And the other interesting thing about ICs is that this is not only true for the MOSFET, this is also true for resistors and capacitors also which are the other two types of devices that we will use assuming that the resistor and capacitors have the same dimensions naturally they should also be the same. There are many different ways of building resistors on an IC, when you say two resistors are identical; you have to use the same type of resistor also.

Having said this, let us come back to this bias circuit and point out that or figure out how the circuit will behave. I think many of you might have seen this in a basic analogue circuits course, but let us nevertheless quickly write down the equations. So, I have called these devices M 1 and M 2; our job is to find out the drain current of the MOSFET; M 2. So, to do that we to find out the drain current; we need to find out the gate source voltage, note that both the devices M 1 and M 2 have the same gate source voltage.

And let us say that voltage is V GS 1 can be figured out for the first device through its current voltage relationship. The drain current for M 1 is nothing, but I naught and this is the gate source voltage for device one. Note that this is also the gate source voltage for device two and therefore, this means that nominally I D 2 is equal to I naught, there are several things we need to realize.

Before we go ahead with some details of the circuit, the first assumption or the first thing to note is that it is not an assumption M 1 is always in saturation; this is because the drain source voltage for M 1 is equal to the gate source voltage and clearly the condition for the MOSFET to go into triode is a go out of saturation into triode is for the drain source voltage should be lower than V G S minus V T and this is clearly not its one threshold voltage away from that. Now the second point is an assumption, we have assumed that M 2 is in saturation because we have applied the same gate source voltage that depends on what the drain voltages.

So, this our assumption is valid only if V D 2 is larger than or equal to V G S 2 minus V T which happens to be the V D sat of the transistor as long as the drains voltage is large

enough to keep M 2 1 saturation. The output current drain current I D 2; will be nominally equal to I naught.

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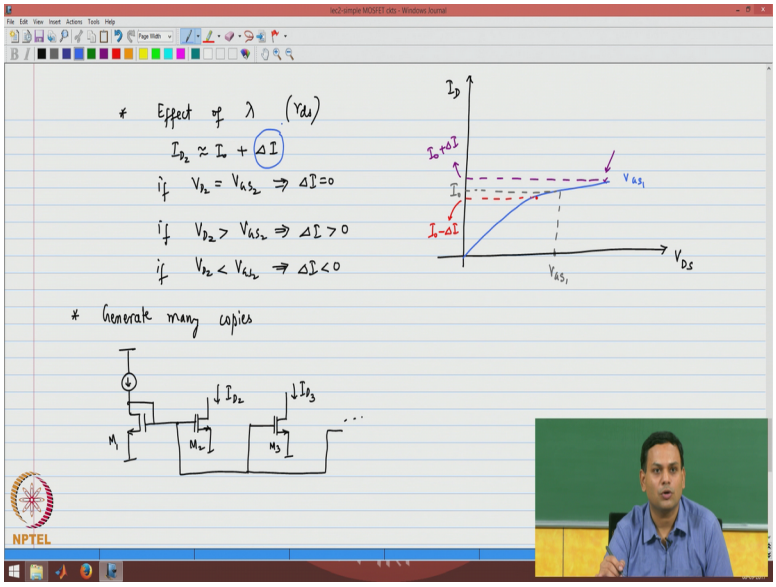

There is a third point to note which is the effect of lambda. So, I D 2 will be nominally equal to I naught, but there will be some delta I depending on the drain voltage. If V D 2 was equal to V G S 2 then delta I is 0; if V D 2 is larger than V G S 2; delta I will be positive and if V D 2, a smaller than V G S 2 delta; I would be negative. And therefore, the output current will be slightly different from the input current.

This is clearly an effect of the R D S of the transistor, in other words if I were to draw the I D versus V D S for the devices. So, I have shown a slight dependence on V D S what I will do? I will exaggerate that dependence to show it in slightly better detail.

Now, on the same curve let us say this corresponded to a gate source voltage V G S 1; this curve on this curve M 1 is located at a drain source voltage equal to V G S 1; this is the operating point of M 1 and that will happen at a current I naught; however, M 2 is also on the same curve, but the drain source voltage can be different.

If the drain source voltage were here for example, clearly the drain current I D 2 is going to be larger than I naught whereas, if it were slightly smaller the drain current would be smaller than I naught; I hope this is clear now. The nice thing about this circuit is that; you can now generate many copies of this current using just a single MOSFET; M 1. I

have generated one copy here, but nothing prevents me from connecting this to as third MOSFET generating a second copy of this current and so on, I can generate as many copies as I want.

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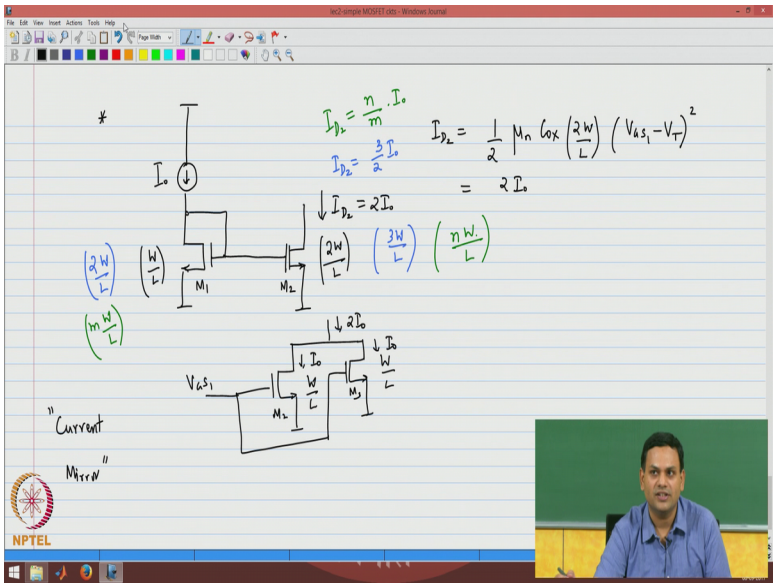

So, the third thing about this is that I can not only generate copies, I can generate multiples of this. Let us say M 1 had a ratio W over L; in other word it had the width W and a length L. If I choose M 2 such that; it has twice the width 2 W and a length L, then I D 2 is given by this relationship; this is clearly 2 I naught. So, therefore, I get twice the current here, this is exactly the same as putting two devices in parallel. Please note that if I put two devices of width W in parallel, that will give me the same effect because each of these has a current I naught and the total current is 2 I naught.

Now, the last thing is that we can also generate fractional currents because for example, I am going to show this on the same diagram in blue colour. If I want I D 2 to be equal to 3 by 2; I naught, then all I have to do is; I have to use a width 2 W for M 1 and I will use a width 3 W for M 2 then I D to becomes 3 by 2 I naught. In fact, if I use M W over L for M 1 and n W over L for M 2, then I D 2 is equal to n over m times I naught, so you can create fractional current. So, this current source is a very versatile current mirror is a very versatile circuit.

Next we will see how this current mirror can be improved to give you better behavior with respect to the drain source voltage. In other words, we want the output current to be

exactly equal to I naught instead of; so in other words we want to get rid of this delta I term as much as possible, we will look at that next.