Analog Integrated Circuits
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Lecture – 19
Differential Amplifier offset

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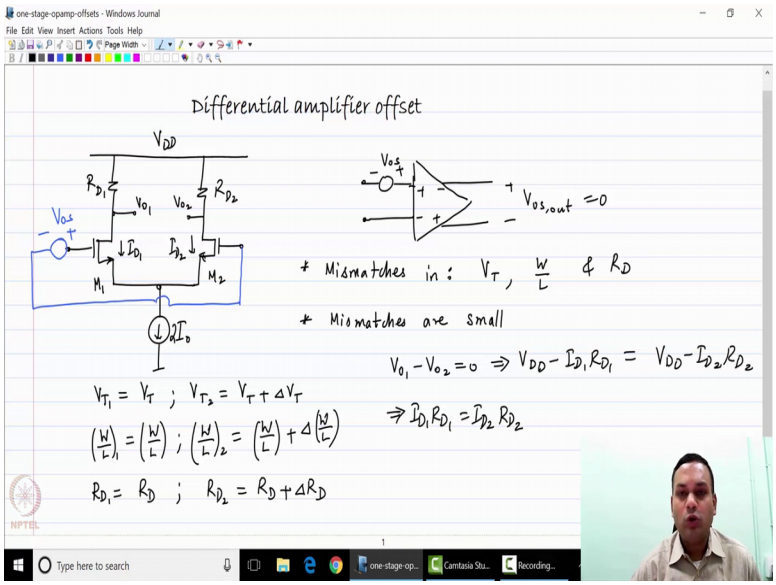

In today's lecture, we are going to study the offset of differential amplifiers, and see how to extend it to opamp offsets. So, let us take the simplest possible differential amplifier, which is a resistively loaded differential amplifier. Let us assume that the load resistance as R, R; the two transistors are M 1 and M 2; and the two currents are I D 1 and I D 2; and the two outputs are V o 1 and V o 2. Now, this as a block diagram can of course, be represented in this form. And if you were to represent the offsets in the circuit the mismatch is in the circuit as an offset voltage you would do it as a series voltage source; and by convention we would use the sign, so that a positive voltage needs to be applied. Now, remember just a reminder V o s the input referred offset is defined as the voltage that needs to be applied to your amplifier such that the output offset is 0.

So, now, let us do that. So, we will assume that the two resistors are R D 1 and R D 2, we will assume that mismatch as exist in V T W over L and r d. So, nominally the two resistors are R D, but in reality they are slightly different we will also assume that mismatches are small. So, these are the two assumptions in our analysis. So, now, we

will say that V T 1 is V T and V T 2 is V T plus sum delta V T, so it is slightly different from V T 1. And we will say W over L of 1 is W over L W over L of 2 is W over L plus delta W over L. Finally, R D 1 is equal to R D and R D 2 is equal to R D plus delta R D these are our assumptions for this amplifier.

Now, we want to find out the if you take such a circuit you want to find out the input voltage that needs to be applied such that the output voltage offset is zero. So, now, let us complete the circuit in that manner. So, I have an input offset voltage that is being applied. So, this is the offset voltage that is being applied to the circuit. And we know that the output offset is 0. So, we know that V o 1 minus V o 2 is equal to 0. Now, this clearly means that the V DD minus I D 1 R D 1 should be equal to V DD minus I D 2 R D 2 and this clearly means that I D 1 R D 1 should be equal to I D 2 R D 2. So, this is another fall out of the definition of offset.

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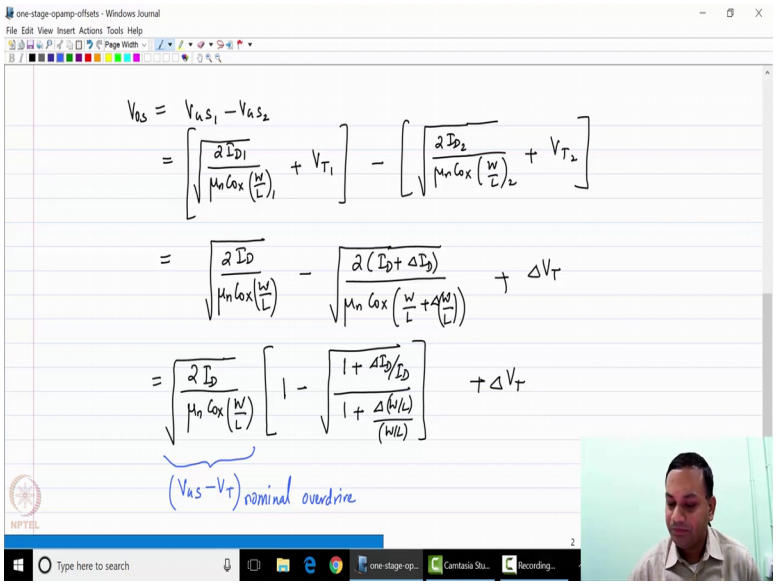

Now, let us write down the expressions for offset. So, clearly if you go through the circuit v o s should be equal to V GS 1 minus V GS 2. And this is clearly equal to root of 2 I D 1 mu n C ox W over L 1 plus V T 1 minus root of 2 I D 2 mu n C ox W over L 2 plus V T 2. We are going to rewrite this expression as root of 2 I D mu n c ox W over L minus root of 2 into I D plus delta I D mu n c ox into W over L plus delta W over delta W over L plus V T 1 minus V T 2, which happens to be delta V T. So, let us now take this expression out of the brackets as a common factor. So, this would be the second factor

would be 1 plus delta I D over I D over 1 plus delta W over L over W over L. So, please note that this particular term here represents the nominal V GS minus V T or V D sat of the device. So, this is the nominal over drive of the devices.

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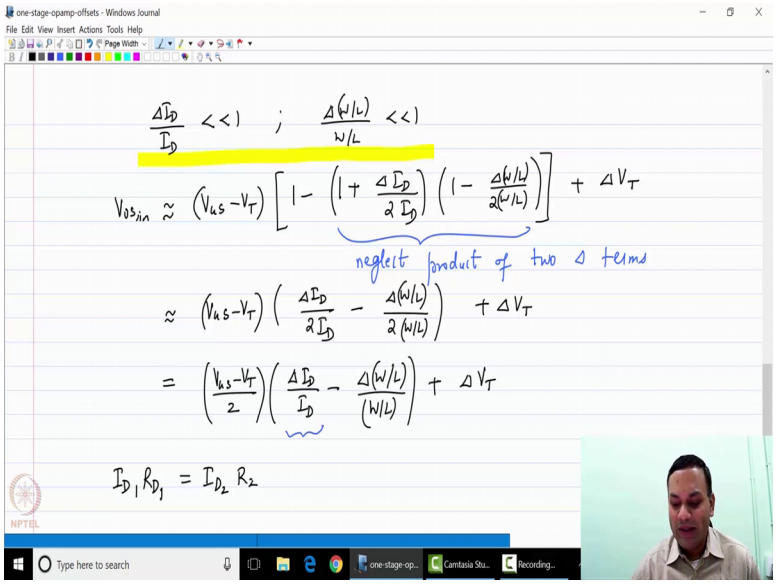

So, now let us simplify this further by using the following assumptions. We know that the mismatches are small, therefore delta I D by I D is much less than 1, and delta W over L over W over L is much much smaller than 1. So, we will make these two assumptions. And once you do this, you can see that the expression for the input offset becomes V GS minus V T times 1 minus so root of 1 plus delta I D by over I D becomes 1 plus delta I D over 2 I D into 1 minus delta W over L over 2 W over L.

Now, we can expand the term here and we will also neglect product of two delta terms. So, we will assume because this is true we will assume that delta I D by I D times delta W over L over W over L is so small that it can be neglected. So, this becomes V GS minus V T into delta I D over 2 I D minus delta W over L by 2 W over L plus delta V T. So, this is of course, V GS minus V T by 2 times delta I D by I D minus delta W over L by W over L plus delta V T.

Now, we realize that the fundamental mismatch is between resistors and between transistors through that V T and W over L. So, this particular parameter is not a fundamental mismatch parameter, and therefore, we need to extract out delta I D by I D in terms of other fundamental parameters. So, I would like to remind you that we derive

previously that I D 1 R 1 should be equal to I D 2 R 2 by definition because the output offset voltage should be 0.

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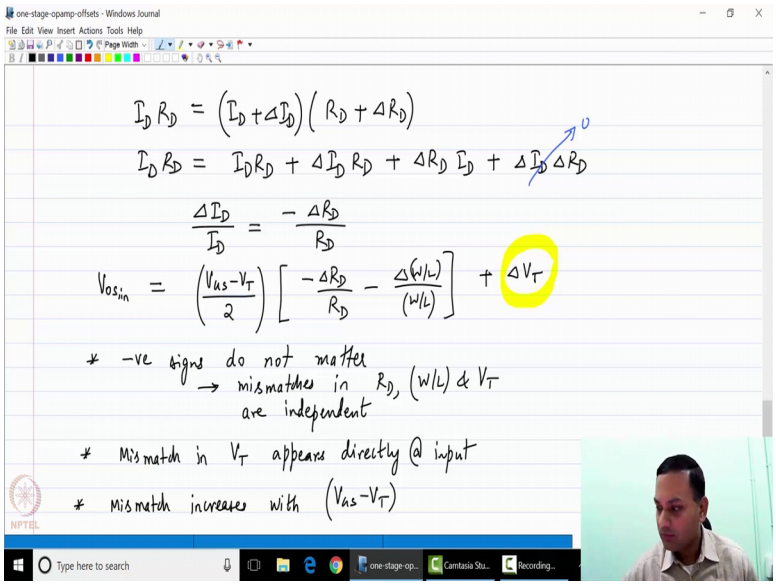

So, this means that I D R D should be equal to I D plus delta I D into R D plus delta R D. So, this is I D R D plus delta I D R D plus delta R D times I D plus delta I D delta R D which we will neglect because it is the product of two terms. Now, this implies that this implies that delta I D by I D should be equal to minus delta R D over R D. So, now, this is actually a fundamental mismatch parameter. So, now, let us go back and plug this in to look at the actual offset voltage of the differential amplifier. So, clearly the offset voltage is this expression here. So, there are several things to note here.

So, first of all the negative signs do not matter because the mismatches that we are considering so mismatches in R D W over L and V T are independent. In other words, if you were to look at the statistics, there may be some chips where delta R D could be positive and that could be some chips where delta R D is negative, and same for delta W over L, and these two moves in totally independent directions. So, what we are actually interested in is the standard deviation of the offset which we are going to write now.

But before doing that we will just note down one more point which is that the mismatch in the threshold voltage appears directly at the input of the differential amplifier. Now, this is quite important. You can see that the mismatch delta V T appears directly without any modification. This means that irrespective of how you design the circuit the currents

and voltages for example, the any mismatch in the threshold voltage would directly appear as an input referred offset. So, therefore, this is expected to be the dominant term. And finally, you should note that mismatch increases with the over drive V GS minus V T, therefore if you want low input referred mismatch due to R D and W over L, you should try to minimize the over drive voltage.

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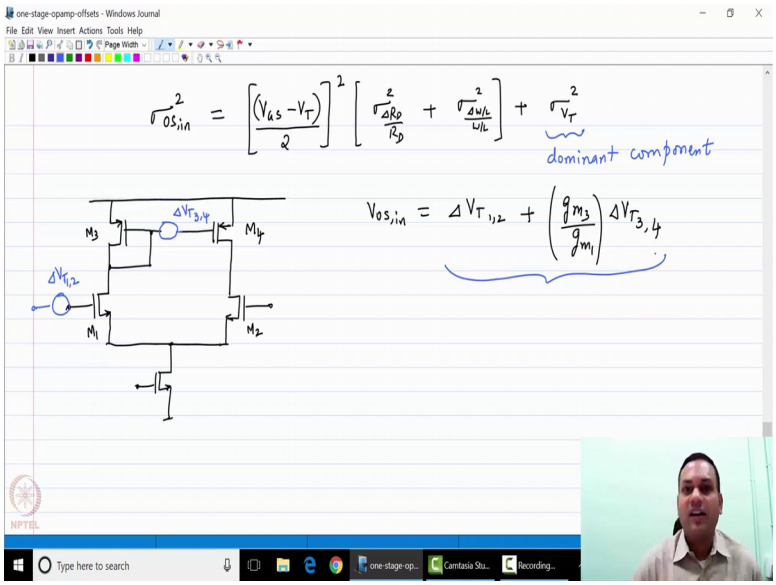

Now, let us try to write down the standard deviation at the input. So, sigma squared o s in is V GS minus V T whole squared V GS minus V T by 2 the whole squared times sigma squared delta R D by R D plus sigma squared delta W over L over W over L plus sigma squared V T. So, this is the expression for the input referred offset of the differential amplifier. And as you can see you expect this to be the dominant component, since it appears directly at the input.

Now, suppose you were to built an a single stage opamp, the input of course is a differential pair, but you also instead of a resistive load, you actually have a current mirror. Now, let us see what would happen if you had a one-stage opamp. Let us consider only the V T mismatch because that is expected to be most dominant. So, as you might imagine the input referred offset in the threshold voltage between 1 and 2 directly appears at the input.

What about the offset of M 3 and M 4, it turns out that this offset can also be represented as a series voltage source delta V T 3 comma 4. And if you look at the input referred

component of this, if you look at the output offset voltage and divided back by the gain, you can clearly see that the input referred offset V o s in would have two components. So, the component from 1 and 2 would be directly delta V T 1 comma 2, but the components from 3 and 4 would be scaled by their relative g ms, I will leave this as a home work exercise for your practice.