Analog Integrated Circuits
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Lecture – 18
One Stage OpAmp-3

In this lecture we will look at the frequency response of the one stage opamp that we have been looking at so far.

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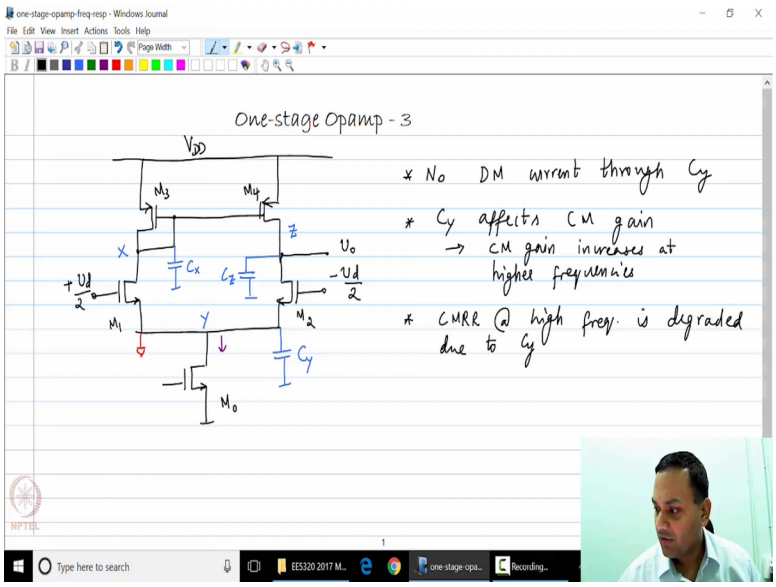

So, to draw the frequency response let us first draw the opamp circuit.

So, this is the circuit of the 2 stage opamp, I am going to number the transistors from M 0 to M 4, let us assume that the opamp is being driven differentially. So, I have inputs of plus v d by 2 and minus v d by 2.

Now, let us assume now that every node of the circuit has some parasitic capacitance. So, we now have 3 nodes in the circuit, I am now going to name them x y and z and; obviously, the parasitic capacitance at these nodes will come from the internal capacitances of the transistors themselves, and once you design the opamp you will know what these capacitance values are.

For now we will just assume they are some capacitance C x, C y and C z. Now what is the effect of C y? Now we will note that C y is actually at small signal ground and therefore, there is no differential mode current through C y and therefore, and of course, this is because both ends of C y are shorted to small signal ground. So, therefore, there is no C y makes no difference to the differential mode picture.

However C y affects the common mode gain of the circuit, clearly the circuit originally expected high impedance looking downwards whereas, the minute you have C y this impedance will look high for low frequencies, but at higher frequencies C y will start presenting smaller and smaller impedances and therefore, the common mode gain which was originally 0 at very low frequencies will start getting higher and higher.

So, I just point out that common mode gain increases at higher frequencies and finally, the CMRR at high frequencies is degraded due to C. Now with that understanding we will move on to the differential mode picture of the circuit, we will now see the effects of C x and C z on the small signal differential mode analysis.

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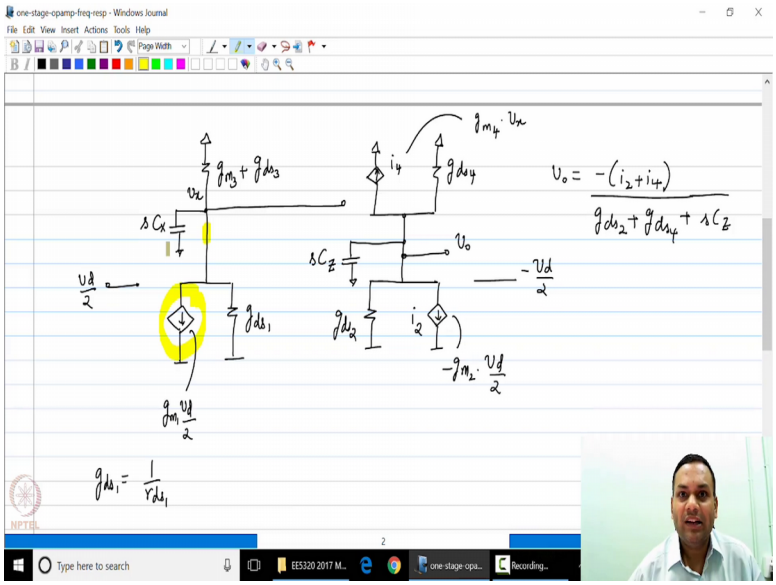

So let us quickly draw the small signal picture.

So, this is g m 1 times v d by 2, and I will now express the resistances as that equivalent conductances. So, I am going to call this g d s 1 clearly g d s 1 is nothing, but 1 over r d s one and so on.

At this node at node x we now have 3 impedances connected up, due to the transistor being due to the drain and gate of transistor M 3 being connected, we find that the impedance that M 3 presents is now one over sorry the conductance that it presents is g m 3 plus g d s 3 this is due to the feedback option.

Now, apart from this you also have capacitance C x to ground the conductor or rather. The component the admittance component of the imaginary component of the admittance is s times C x.

Now, this generates a voltage v x at this node and this v x is now applied to the gate of transistor M 4, and that causes a small signal current i 4. And you also have the component from transistor M 2 and this is nothing, but the current source i 2 is nothing, but g m 2 times v d by 2 with a negative sign this conductance is of course, g d s 2 and this is g d s 4. Current i 4 is nothing, but g m 4 times v x and finally, you have a capacitance C z connected between the output loop and this is the output voltage.

So, now we can start looking at the at the signal progression through the circuit. So, let us first look at the output node. So, we can now see that voltage v o is created by these 2 currents flowing into these 3 impedances.

So, we will write v o to be equal to I am going to call this current i 2 is minus of i 2 plus i 4 this is the total current flowing into the node times the sum of all the impedances in the node, or it is 1 over some of all the admittances because they are all in parallel. So, that is nothing, but g d s 2 plus g d s 4 plus s C z.

Now, it is our job now to find out i 2 of s and i 4 of s. So, let us now write the expression for i 2 of s.

I 2 of s is clearly minus g m 2 times v d by 2.

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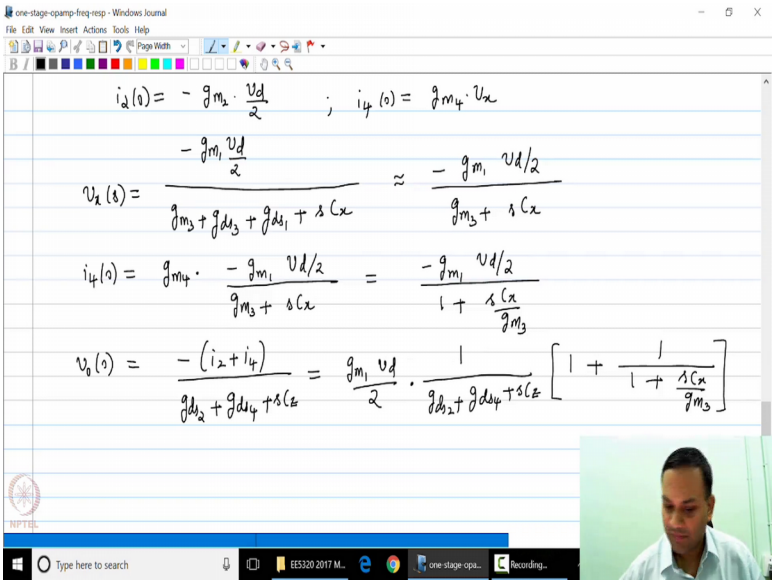

And please remember that g m one is equal to g m 2, g d s 1 is equal to g d s 2 g m 3 is equal to g m 4 and g d s 3 is equal to g d s 4. We are assuming that the 2 transistors on either side of the line of symmetry are identical.

Now, let us find out what i 4 is to find out i 4, i 4 is nothing, but g m 4 times v x we now need to find out what v x is.

So, i 4 is or i 4 of s is g m 4 times v x, and now it is our job to find out v x of s. V x of s is clearly equal to this current multiplied by the total impedance at that node with a negative sign. So, now, I will write this as the negative of g m 1 v d by 2 this is the total current flowing into the node times the sum of all conductances at that node, I mean over the sum of all conductance at that node

Now, the sum of all conductances at that node is of course, g m 3 plus g d s 3 plus g d s 1 plus s C x. And since we know that normally g ms are much larger than the corresponding g d s s, I will approximate this to minus g m 1 v d by 2 over g m 3 plus s C x.

Now, finally, we are in a position to write the expression for i 4 of s, i 4 of s is now g m 4 times minus g m 1 v d by 2 over g m 3 plus s C x, I am now going to write it in a very specific form I am going to say this is minus g m 1 v d by 2 over 1 plus s C x over g m 3,

this is because g m 3 is the same as g m 4. And now the output voltage v o of s we have seen that it is minus of i 2 plus i 4 over g d s 2 plus g d s 4 plus s C z.

This is clearly g m one v d by 2 over 1 over g d s 2 plus g d s 4 plus s C z times 1 plus 1 over 1 plus s C x over g d 3.

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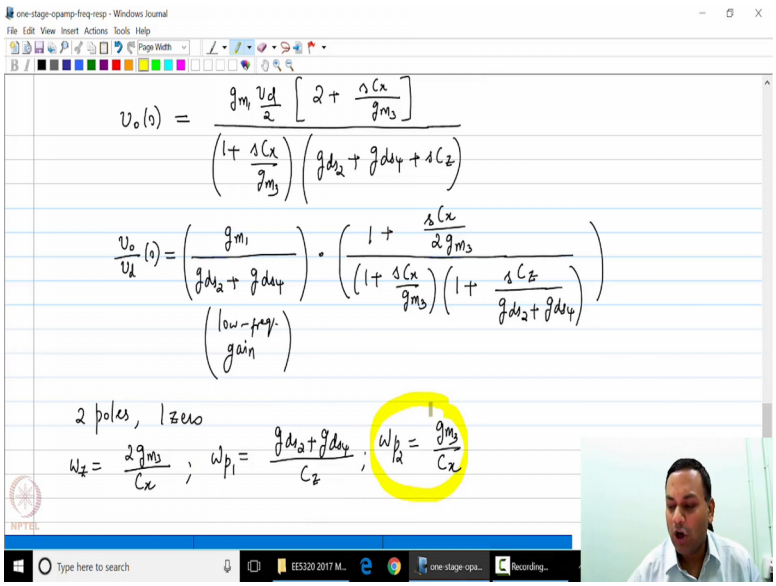

So, finally, v o of s is g m 1 v d by 2 times 2 plus s C x over g d 3 by 1 plus s C x over g m 3 times g d s 2 plus g d s 4 plus s C z.

Now, I am going to write this in a standard form, I want to rewrite this as v o by v d of s. So, this is the gain of the circuit, I want to write this in a standard form where I have 2 components the first component should correspond to the low frequency gain, and the second component should go to one at low frequencies, but should contain the poles and zeros of the system.

So, now let us rewrite this in that specific form. So, I am going to take the component g m 1 over g d s 2 plus g d s 4 out of this expression because this is the low frequency gain of the circuit, and this is going to be the frequency dependent part. So, the system has one 0 at 2 g m 3 over C x and it has 2 poles the first pole is at 1 plus is at g m 3 over C x and the second pole is at g d s 2 plus g d s 4 over C z. So, the system has 2 poles and one 0. So, that is the first thing we will understand and the second thing to realize is that the positions of the poles and zeroes. So, omega z is at 2 g m 3 over C x, the first pole omega

p one is at g d s 2 plus g d s 4 over C z and the third pole sorry the second pole is that g m 3 over C x.

Now, let us see if these things make sense. So, first of all you can see that g d s 2 plus g d s 4 is the smallest quantity and therefore, this pole is the closest pole is the smallest pole and therefore, this is going to be the dominant pole of the system. Now you can see that that dominant pole depends on the output conductance g d s 2 plus g d s 4 is the overall output conductance of the system, over the total capacitance at z which is the sum of the device capacitance and the load capacitance.

omega p 2 is the second pole in the system and that comes about because you have the gate capacitance of the of M 3 and M 4 hanging at the common gate domain, that will be the dominant capacitance at that mode, this pole is often called the mirror pole.

Now, please note that you now have a 0 at twice omega p 2, the 0 frequency is at twice omega p 2 and first of all you need to ask yourself why you see a 0.

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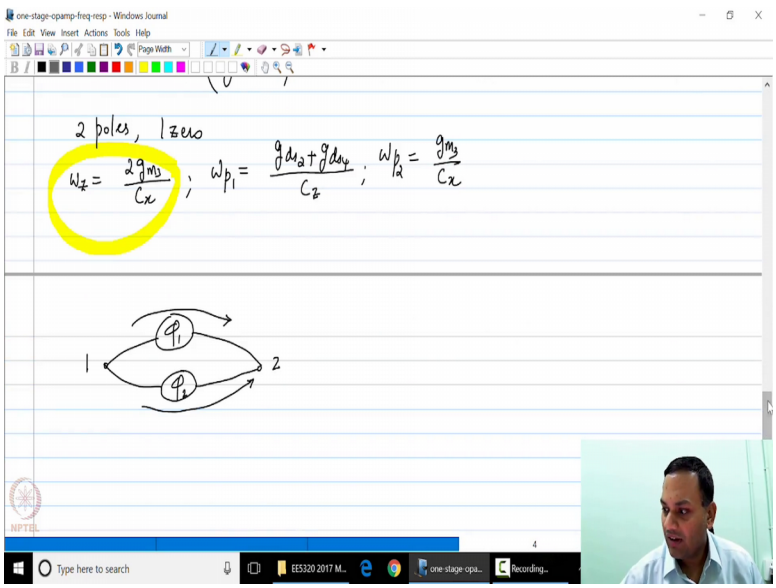

Normally you will find that you see a 0 when you have when you look at the transfer function between 2 paths, if you see a relative phase shift especially a frequency dependent phase shift between the 2 paths you will normally see a 0.

So, that the 2 through the 2 paths the signal adds destructively at a particular frequency do we have these 2 paths in the system? It turns out that we do if you actually look at the

path travels by the signal there are 2 paths travels by the signal, in the first path so, the signal from minus v d by 2 travels directly to the output node. The signal from plus v d by 2 takes a different path where it sees an extra phase shift due to the presence of C x, and that is why you see the additional 0 in this path and it turns out that the frequency of the 0 is at twice the frequency of the pole.