Analog Integrated Circuits
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Lecture – 17
One-stage OpAmp-2

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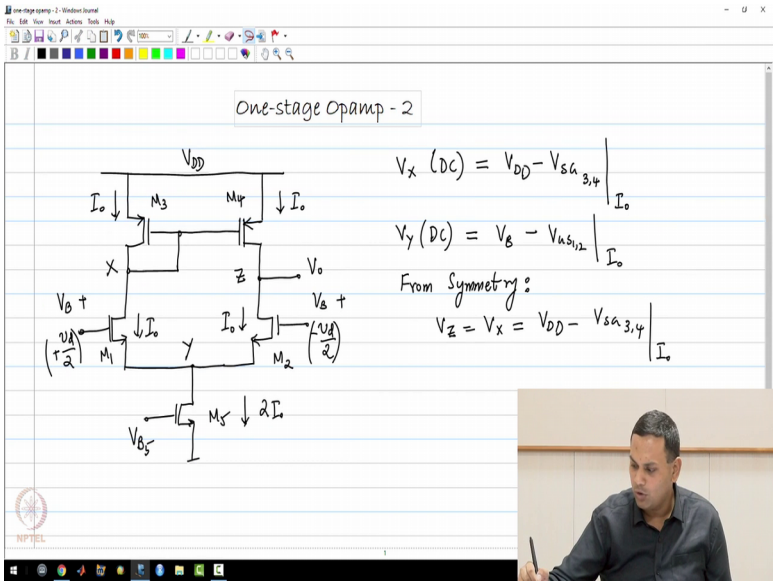

In this lecture, we are going to look at the one-stage opamp that we saw previously in a little bit more detail. So, as we saw earlier the one-stage opamp consists of five transistors. So, these five transistors are M 1, M 2, M 3, M 4 and M 5. So, these are the five transistors. And we saw earlier that M 5 carries a current 2 I naught and purely because of the symmetry between M 1 and M 2, there will be a current I naught through each of these two sides, and the output is taken at the drain of M 2.

Now, let us look at the dc picture in a little bit more detail. So, clearly if M 1 and M 2 have bias current of I naught each, the bias current of M 3 and M 4 is also I naught each, because there is no current through the gates of M 3 and M 4. And the bias point at node x which is the drain of M 1 happens to be the V x DC and this will be the supply voltage V DD minus the source gate voltage of three or four; and this source gate voltage remember is calculated at a bias current I naught. So, the bias points of M 1, M 2, M 3, M 4 are calculated with a bias current I naught; the bias point of M 5 is calculated with a bias current of 2 I naught. So, node x is at a voltage V DD minus V SG 3, 4.

Now what about let me call the common source node of M 1 and M 2 as node y. So, node y, and I will also call the output as node z, because we will be coming to that next. So, we need to find out the bias voltage at node y to do that we need to do something about what voltage is applied to the circuit. So, I am going to say that the input has some v b bias voltage and a differential voltage V d by 2 and minus V d by 2 applied to the to the two halves.

Now, if you look at the if you look at the two sides from a bias point of view, now you see that all bias voltages should ideally be symmetric and the two transistors have the same current and therefore, should have the same V GS voltage V GS 1 will be the same as V GS 2. And therefore, V y should be V B minus V GS 1, 2 at a current I naught, this will be the DC voltage at node y. And purely from symmetry, if everything is matched between the two halves of the circuit we can say that V z will be equal to V x will be equal to V DD minus V SG three 4 at a current I naught. This is purely from symmetry; in reality, the DC voltage at node z will be set by DC negative feedback around the opamp. Now, we have now said that DC operating points of all transistors, we know the V GS, we know the V DS we know the bias currents now let us look at the two other important DC parameters of interest, what is called the input and output common-mode range.

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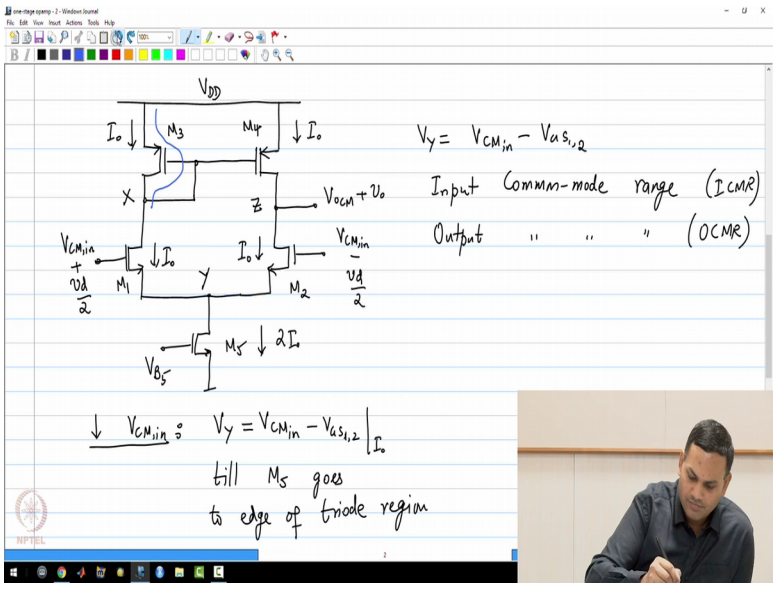

So, now since the input bias voltage is common between both sides the average voltage between the two inputs is now, going to be the common-mode voltage in this case as I have drawn it I am going to call it V CM in which is the same as v bias which I drew in the previous page. This is the input common-mode voltage, on top of which I have a differential signal that is being applied. Now, of course, in this scenario V y is equal to V CM in minus V GS 1, 2. And clearly you can see that what I have called as V CM in is the same as the DC voltage V B that I had drawn on the previous page.

Now, I need to find out a quantity called the input common-mode range and which is I am going to abbreviate it by ICMR; and the output common-mode range and I am going to call that OCMR, just for brevity. Now, assume that the average voltage at the input is changed it can be either decreased or increased, I want to find out what the absolute limits are for this particular input common-mode voltage V CM in; and I can say the same thing for the output common-mode voltage VOCM or the output common-mode value.

Now, suppose I start decreasing V CM in, as you can see if I decrease V CM in the as long as M 5 has a very large output resistance its current 2 I naught will not change too much, and the two transistors M 1 and M 2 will still carry the same current I naught. And an immediate consequence of this is that they will have the same gate source voltage, and therefore, V y will follow V CM in, but with a difference of V GS 1, 2 at a current I naught. This will happen till M 5 goes to the edge of triode. So, if I keep reducing the input average value, the value of V y will follow it directly because M 5 even for changes in the drain voltage M 5 keeps the current constant it is meant to be a current source. And therefore, V y will follow V CM in, but this will happen only till M 5 is in the saturation region. The minute it goes into the triode region, any change in V y will cause a large change in I naught. So, till that happens the circuit will behave properly and the g m, r d s etcetera of M 1, M 2, M 3, M 4 will be maintained.

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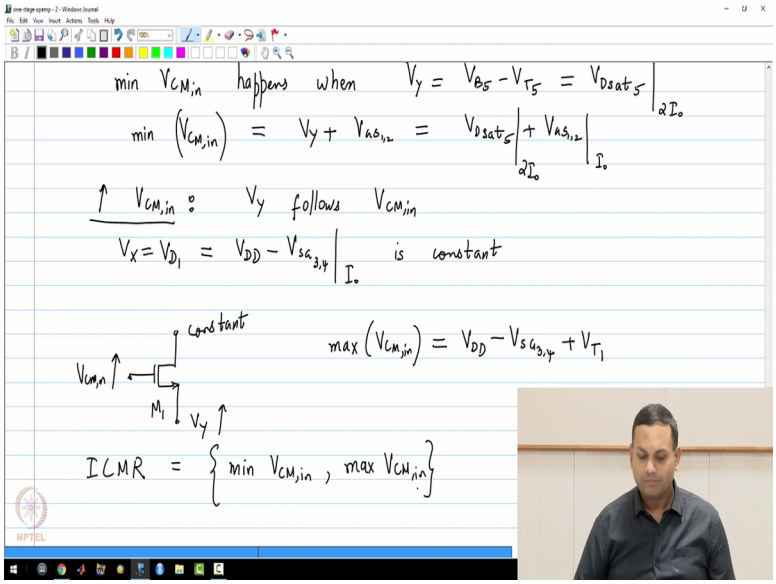

So, the minimum value of V CM, the minimum value of V CM in will happen when M 5 is at the edge of triode region; and at that point V y is equal to V B 5 minus V T 5. And this voltage because there is no signal component this also happens to be V D sat of M 5 calculated remember at a current 2 I naught. At this point the two currents in M 1 and M 2 the currents in two transistors M 1 and M 2 is still I naught each; and therefore, the minimum value of V CM in is equal to V y plus V GS 1, 2 which is nothing but V D sat 5 plus V GS 1, 2. Again I just wanted to point out that V D sat 5 is calculated at a current 2 I naught, whereas V GS 1, 2 is calculated at a current I naught because these are the respect of bias points. So, the input common-mode voltage cannot be below this value.

Now, next we will see what happens if you start increasing V CM in. If this happens of course, V y still follows V CM in, but the nice thing about this is that V y is now going to increase. And when this happens M 5 goes further and further away from the triode region which works well for us. So, M 5 there is no problem with transistor M 5. But let us quickly look at transistor M 1, if you look at the drain voltage of transistor M 1, this is actually V DD minus V SG 3. So, as you can see V DD minus V SG 3 is the voltage at node x. So, V x is V D 1 is V D 1 and that is nothing but V DD minus V SG 3, 4 of course, at a current I naught.

Now, if I change V CM in, the current source M 5 keeps the total current at 2 I naught; and the currents through each branch still I naught, and therefore, this voltage is constant.

And now you have a situation where for transistor M 1, I have the three voltages the gate voltage is V CM in which is increasing, V y is also increasing at the same rate, so that it maintains a constant V GS, but this voltage is constant. Therefore, eventually transistor M 1 will hit the edge of the triode region and this tells us that the maximum value of V CM in the input common-mode will happen when M 1 is at the edge of triode region. And that will happen when the gate voltage is exactly one threshold voltage above the drain, so that will be V DD minus V SG 3, 4 plus V T 1.

Now, the input common-mode range is clearly the range of input common-modes for which the circuit behaves properly, and all transistors are in saturation. And this happens to be a voltage which is minimum V CM in to maximum V CM in, this range of voltages is called the input common-mode range. What about the output common-mode range that is a little bit easier to see.

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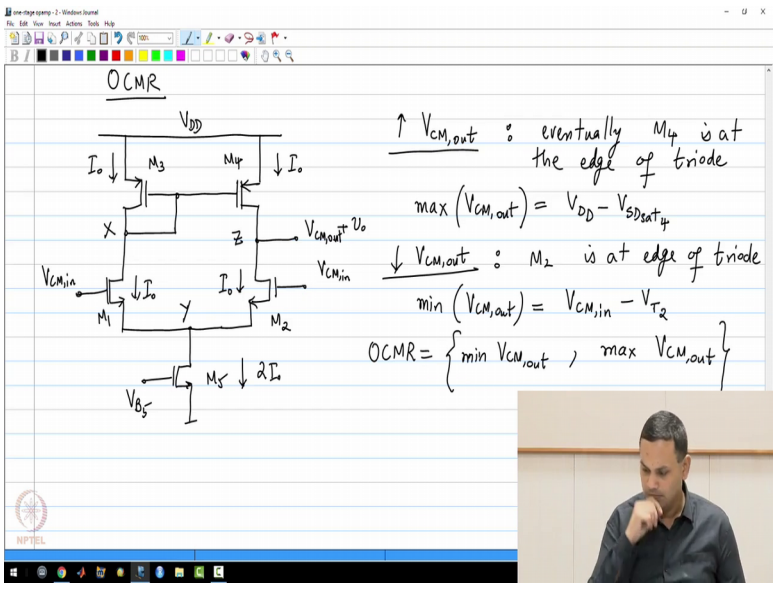

If I take this circuit, and look at its output. So, I am going to call that V CM out or V CM out. So, the maximum value of V CM out happens when M 4 is at the edge of triode region. So, if you try to increase V CM out, eventually M 4 is at the edge of triode and this will happen at a voltage maximum value of V CM out when this is exactly V DD minus V SD sat of M 4. Because that gate of M 4 which is V x is at V DD minus V SG the drain can go one threshold voltage above the gate because it is a PMOS transistor and

this will be the voltage which can be which this will be the maximum voltage at the output that can be achieved without sending M 4 into triode.

Now, what happens if you decrease V CM out, if you do this, you can see that the gate of M 2 is held at V CM in and remember for the common-mode we are not looking at V d at all, we are not looking at the swing limits this is more of a common-mode range thing. So, the minimum value of V CM out will be achieved when M 2 is at the edge of triode. And this will happen at a voltage when the drain of M 2 goes one threshold voltage below the gate and the gate of course, is at V CM in, remember that the opamp will have a particular common-mode anywhere in the input common-mode range. And once you have chosen the input common-mode range, the output can go only one threshold voltage below the input common-mode value. And now of course, the output common-mode range of the circuit is this range, which is minimum value of V CM out to maximum value of V CM out this is the output common-mode range of the opamp. So, these are the two other important DC parameters of the opamp.