Analog Integrated Circuits
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Lecture – 16
One Stage OpAmp-I

In this lecture, we are going to put together some of the circuit that we have learnt so far to build one of the simplest types of CMOS opamps, and which you will see that we will eventually call it the one stage opamp.

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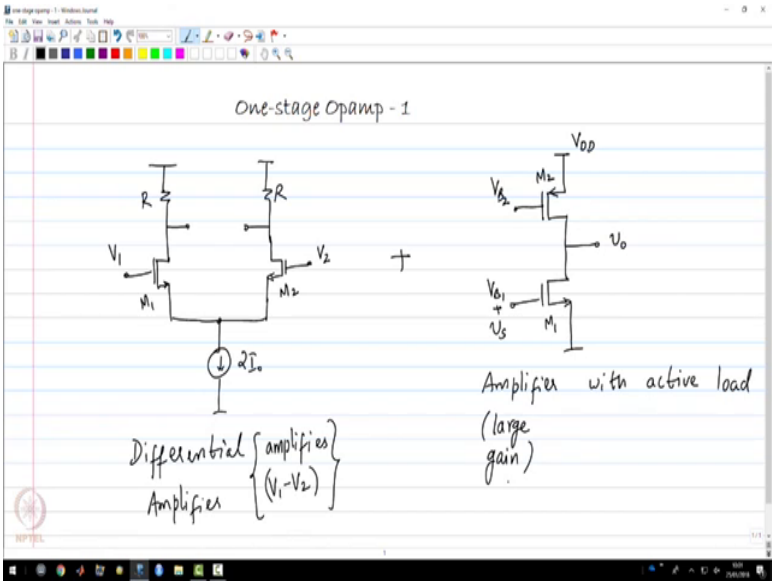

So, we have studied differential amplifiers before. So, the differential amplifier consists of 2 completely identical portions, and from the common source node you have a current source that biases both transistors M1 and M2. The inputs are applied to the 2 gates I will call them V1 and V2. The outputs are of course, taken as the difference between the voltages at the drain.

So, we are going to put together the differential amplifier with the concept of an active load. So, the active load consists of an amplifying device M1, to which you apply a bias voltage, and an input voltage and the output is taken at it is drain, and at the top you have a current source which is represented by a PMOS transistor whose gate M2 whose gate is biased at a voltage appropriately at VB2.

Now, what is the advantage of the differential amplifier? So, the advantage of the differential amplifier is that it amplifies V1 minus V2 preferentially. So, it does not care about the absolute values of V1 and V2, but it amplifies only V1 minus V2. If you look at the V1 plus V2 portion of this particular circuit the amplifier tends to reject it, if you take the ideal case when the current sources has infinite output resistance this transist; this amplifier differential amplifier will completely reject the common mode at it is input. Now this particular circuit is an amplifier with an active load.

This circuit is an amplifier with an active load. What is the advantage of using an amplifier with an active load? The advantage is that you get very large gain from the circuit; compared to a resistive amplifier. So, we are going to put these 2 together to come up with a circuit that will do both differential amplification and give you very large gain and that will be the circuit shown in this particular page.

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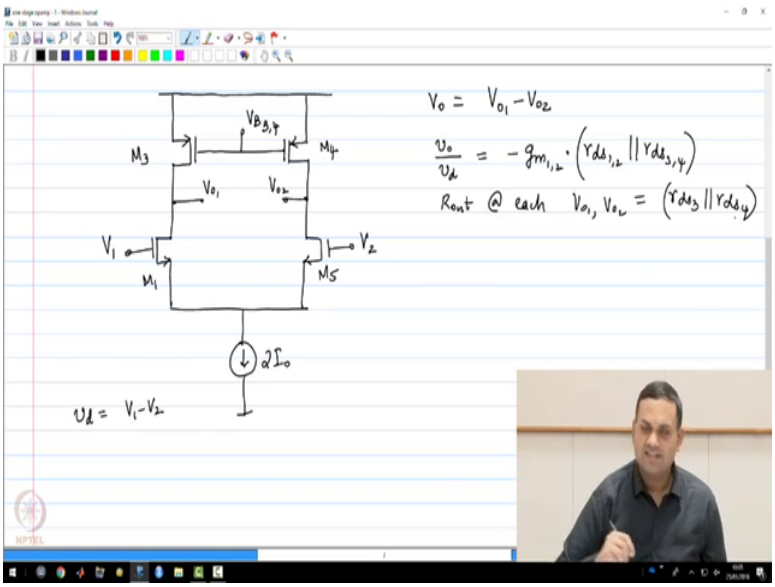

I have taken the differential amplifier and I have removed the resistors and put in an active load.

This is a 4-transistor amplifier which combines the advantages of both the circuits we just saw previously. Now if you look at the output as the difference between VO1 and VO2. The small signal gain of the circuit which is V0 by Vd where, Vd is V1 minus V2 which is the differential voltage applied at it is input. The gain of this circuit is minus g m of 1 and 2 times rds of 1 and 2 in parallel with rds of 3 and 4. So, this gain is the same as that for the active

load of the common source amplifier with the active load, but the advantage is that this circuit will also reject the common mode at the input. Now what do we need from the opamp

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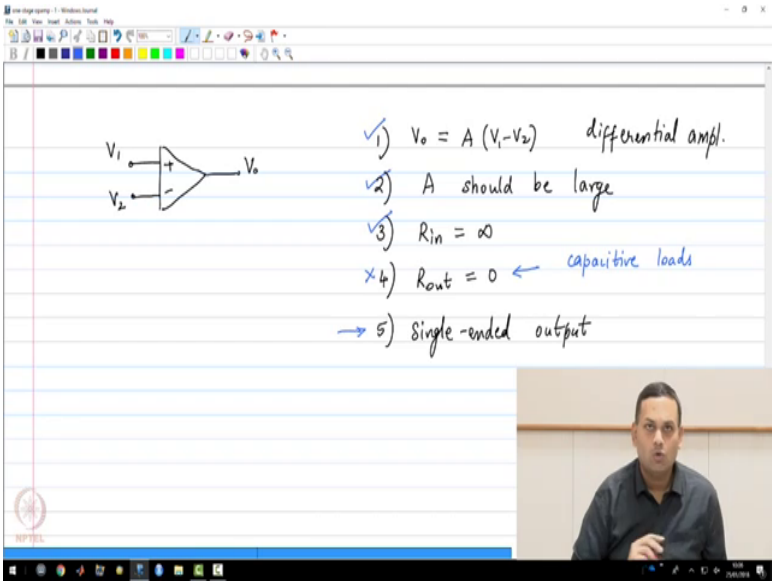

Now, let us go back to the block level conceptualization of the opamp. So, the things we need from the opamp are large gain. So, V0 is some A times V1 minus V2. So, we want A to be very large. We want differential amplification. So, the opamp amplifies only the difference between V1 and V2 and of course, we want Rin to be infinity we want Rout to be 0. So, these are the things that we want from an ideal opamp.

So, turns out the circuit of course, the fifth one is that you need a single ended output. So, the circuit that we have seen so far does differential amplification, and it has large gain right as much as you can get from a single transistor which is very close to the intrinsic gain of a single transistor, it also happens to have r n equal to infinity.

So now we will look at the other 2. So, first of all it turns out that it is very rare to have Rout equal to 0 or something very small and a very small impedance at the output of CMOS opamps in general; the reason is because most opamps drive capacitive loads in which case as long as the output is driving a capacitive load you will find that the Rout does not need to be small for the output to settle to the final value and therefore, we will give up on number 4.

As you can see the circuit that we have come up with happens to have very large output resistance and that is the reason why we are going to give up the output resistance condition.

So, the output resistance at each node; is clearly rds 3 parallel rds 4 this is actually a large output resistance.

Now, we are going to look at the fifth one; which is the condition for single ended output we somehow need to make this opamp have a single ended output, to do that we need to start looking at the signals inside the opamp.

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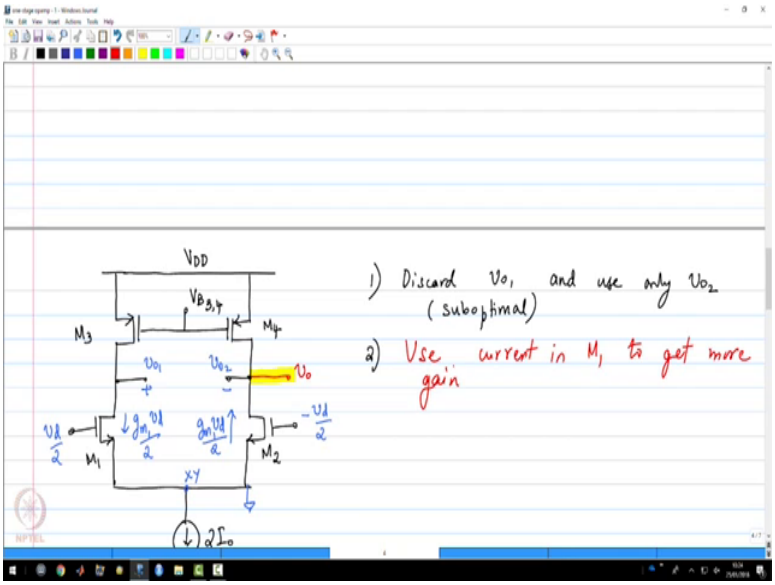

So now, let us assume that you are adding a small signal input differential input. So now, I am going to replace these with small signal quantities. So, I am applying Vd by 2 minus and minus Vd by 2, and for small signals this particular node is at small signal ground and you get outputs VO1 and VO2 and the output is a difference between these 2.

What is the best way of taking a single ended output? Now, there are several different possibilities; the first possibility that we can consider is you just discard V01 and use only VO2. So, what I am saying is you ignore one half of the circuit and take this as the output of the opamp, and it turns out that this will be fine, but you have signal currents flowing through the left half of the circuit s you have gain from the left half of the circuit that you are completely ignoring. So, this is not the best possible way to do this this is definitely suboptimal. So, we do not want to do this.

So, we now need to draw the signal currents and try to figure out how to use the signal on the left-hand side also; now let us assume that I am going to take the output only from the right-

hand side I am going to call that V0. Now if you draw the signal currents inside the circuit we will get a better understanding of what you need to get a single ended output. So, since the X Y node is the small signal ground, the current through the transistor is going to be gm1 times Vd by 2 flowing downwards. And as we saw earlier the current through M2; I am sorry this should be M2 the current through M2 is minus gm1 Vd minus gm2 Vd by 2 flowing downwards or gm1 Vd by 2 flowing upwards.

Now, where does this current flow? Clearly, this current needs to flow through some path as I have drawn it the circuit does not give us any insight as to where the current flows, if we draw the small signal equivalent circuit you will get a better picture. So, we are going to do that next. So, if I draw small signal equivalent for this circuit.

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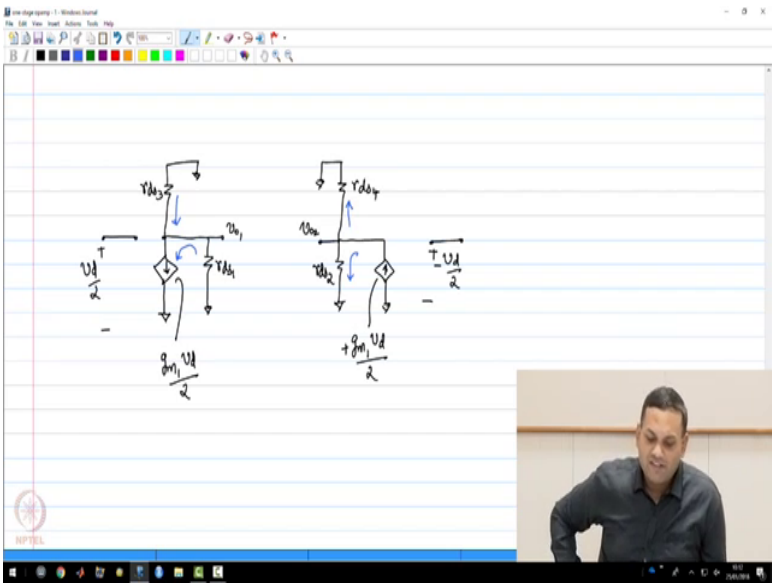

So, this is M1 and I am applying Vd by 2 for M1. So, this is gm1 Vd by 2 and this is rds1

And similarly, on the other side of the differential amplifier, I have M2 transistor M2. So, this is gm2 minus gm2 Vd by 2 and since gm2 is the same as gm1 I will write it as gm1 Vd by 2. And this is rds2 which is the same as rds1. And minus Vd by 2 is what is applied between the gate and source of M2. So, the drain of M1 is now connected to M3 and as we know M3 only has a bias voltage at it is gate. So, this PMOS transistor will not have a gm component it is gate and drain, gate and source are connected to small signal ground. So, the voltage control current shows the gm portion of the PMOS transistors will be 0 and therefore, it will present purely resistive impedance at this node. So, this is rds3.

And similarly, you have rds4 connected to VO2. So, this gives us a better picture of what is happening. So, this is V01 and this is VO2 as you can see the signal current gm1 Vd by 2 and gm2 Vd by 2 actually flow through a combination of rds1 and rds3 on the left-hand side and of course, I can now change the direction to give a better idea. So, if I make this plus Vd by 2 that is a current source flowing upwards and that is a current that flows through rds2 and rds4; to create voltage VO2 and V01. Now, this kind of gives us a better idea of what is happening let us go back to the transistor level picture.

Now, we want to take the output at this node. So, we somehow want to take the signal current in the left half portion and push it into the VO2 node or now the new V0 node. So, as you can see the current needs to be pushed, because it needs to be additive with this current; this is the current being pushed into V0 node from M2 we need to somehow take the current from M1 and also push it into that node. And note that the direction of M1 is such that this current is flowing downwards through M1.

Now, it turns out without going into a very long-winded expression it turns out that the easiest way of doing this is to modify the circuit very slightly.

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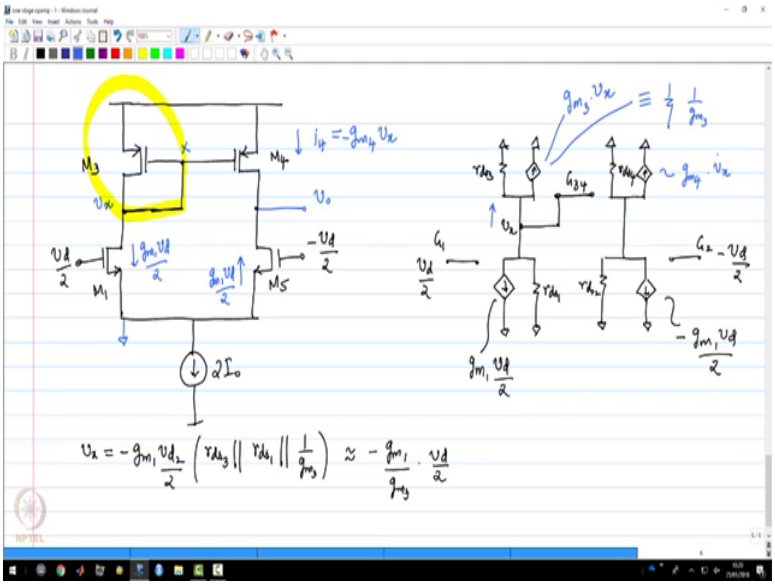

So, instead of using an external normally you would to bias vb3 and vb4 you would need an external current source through a diode connected transistor and we are going to dispense with that connection, and change this connection slightly to modify our circuit. So, please note the change in circuit connection.

I am now taking the gate of M3 and M4 and connecting it to the drain of M3, let us see what happens for the differential currents in this case. Now, as we know the current through this transistor is gm1 Vd by 2 flowing upwards that is flowing into the output node VO.

Now, let us look at what happens to the current through M1. So, this current through M1 which is gm1 Vd by 2 flowing downwards will now flow through M3 and we need to find out what happens to this current this will of course, flow through M3 and because of this connection here there will be a voltage developed at the at that node which has been highlighted here.

Again, you will be able to see this if you draw the small signal equivalent circuit which we are going to do presently, but the point is that this node will now have some small signal voltage I am going to call that node x. This node is going to have a small signal voltage Vx that is developed and this is going to cause a small signal current to flow through device M4, I will call that small i4 will be nothing but gm4 minus gm4 times Vx flowing downwards or gm4 times Vx flowing upwards purely from the transconductance of M4.

Now, let us draw the small signal equivalent circuit and figure out what that voltage Vx is and what that current i4 is.

These are the small signal equivalent circuit for the 4 transistors with the additional condition that; the common gate terminal of M3 and M4 are shorted to this drain. So, this is G34, this is G1 and this is G2. And now these are the output resistances rds1, rds2, rds3 and rds4. And the transistor M1 has a small signal current which is gm1 Vd by 2 flowing upwards, flowing downwards this transistor has a current minus gm1 Vd by 2 flowing downwards.

And this current is going to generate a voltage Vx. And we need to find out what this voltage Vx is. So now, we are I will because I do not want the analysis to get too complicated I am going to use something which all of us should know from before; which is the fact that if I have a transistor whose gate and drain are connected I know that the impedance seen at the gate and drain node is happens to be very close to 1 over gm of the transistor.

In other word, what I should get from my analysis; is that the impedance looking upwards the impedance presented by M3 at node x it should be equal to 1 over gm3, but now as you can see this happens to be a current that is gm3 times Vx. And that should show you that this is actually a resistor of value 1 over gm3.

We have seen this before when we were looking at much simpler circuits. So now, we have a better idea of what Vx should be; Vx of course, should be the current gm1 Vd by 2; flowing into the parallel combination of 3 resistors which are rds3 in parallel with rds1 in parallel with 1 over gm3.

And now, since gm3 would normally be 1 over gm3 would normally be much, much smaller than rds1 and rds3, I will now make an approximation; sorry, there should be a negative sign here, I will now make an approximation that this is approximately gm1 by gm3 times Vd by 2. So, voltage at node x will be the current generated by M1 flowing through the parallel combination of these 3 resistances. And now it so happens that one of those resistances which is 1 over gm3 is much, much smaller compared to rds1 and rds3 and therefore, this expression can be written up.

Now, what happens to this small signal? What happens to this small signal? Voltage that is developed this will now cause a current to flow through M4. So, this current flowing upwards is now gm4 times v g s which is Vx. So, i 4.

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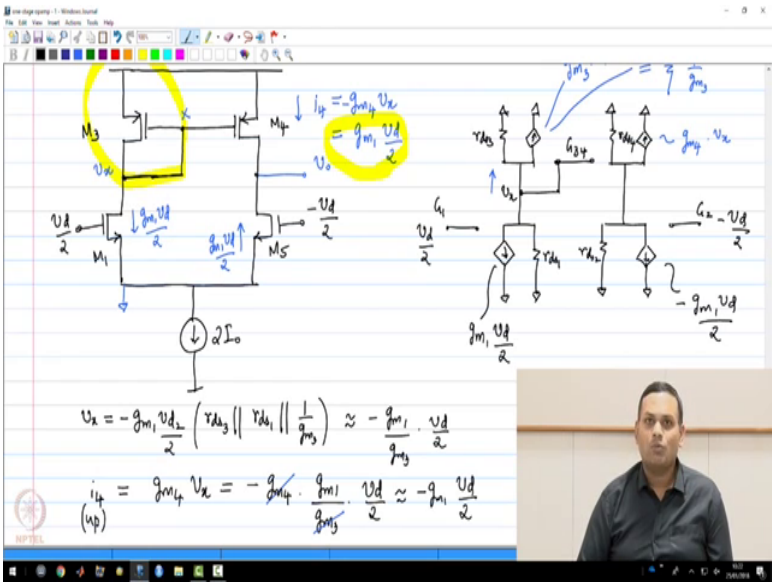

The small signal current through M4 is now gm4 Vx flowing upwards which happens to be minus g m4 into g m 1 by gm3 into Vd by 2 and.

Since the 2 sides are identical g M4 is equal to g M3 and therefore, this is approximately minus gm1 Vd by 2 flowing upwards; please note the direction which means I now have a

current flowing downwards through M4 of value gm1 Vd by 2 flowing downwards and I have now written that in yellow I have written that in blue.

So now it turns out the voltage at node Vout is now equal to.

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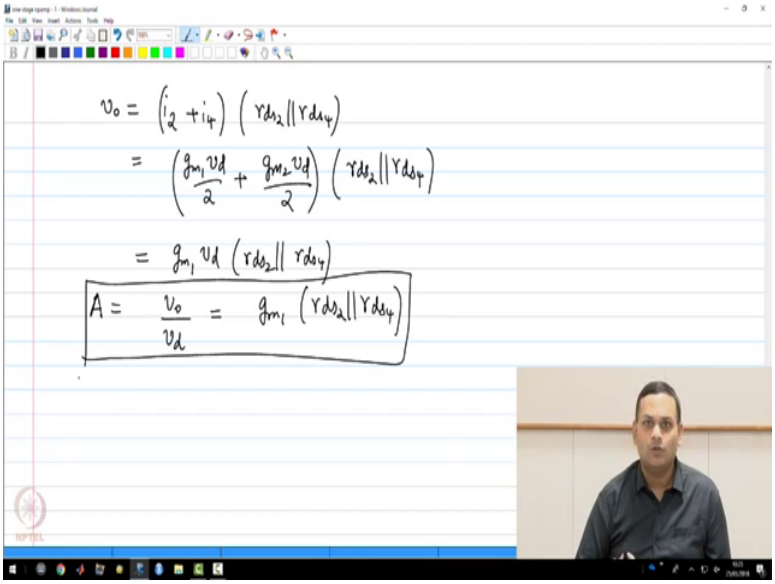

Is now equal to the sum of all currents flowing into that node. So, which is i2 plus i4. So, I have now changed the direction. So, note that i4 is flowing downwards. So, this is the upwards current and the downwards current shown in the figure is now gm1 Vd by 2.

And VO at the output node is the sum of these 2 currents times the impedance which is rds2 parallel rds 4. So, this is nothing but, gm1 Vd by 2 plus gm2 Vd by 2 into rds2 parallel rds4 and since gm1 and gm2 are the same I can now say this is gm1 Vd into rds2 parallel rds4

Now, this tells me that the gain of the amplifier is VO by Vd, this is nothing but gm1 into rds2 parallel rds4 with a positive sign this does not have a negative sign anymore, and now this is the circuit that we have been looking for because it happens to have very large gain very close to the very close to the intrinsic gain of the transistor, and we have managed to get single ended output now. We have now managed to achieve this particular condition also, and the nice thing about this is we have now used the current in M1 we have not discarded it and we have used it to get more gain than 1.

So now we are using all parts of the circuit without discarding any signal currents without wasting any extra power or circuitry and we have achieved pretty much everything that we wanted from an from an opamp.

Now, it turns out that this circuit is now called a one stage opamp, now there is only one final addition to make for this circuit which I will now show. So, let us draw the circuit in it is entirety.

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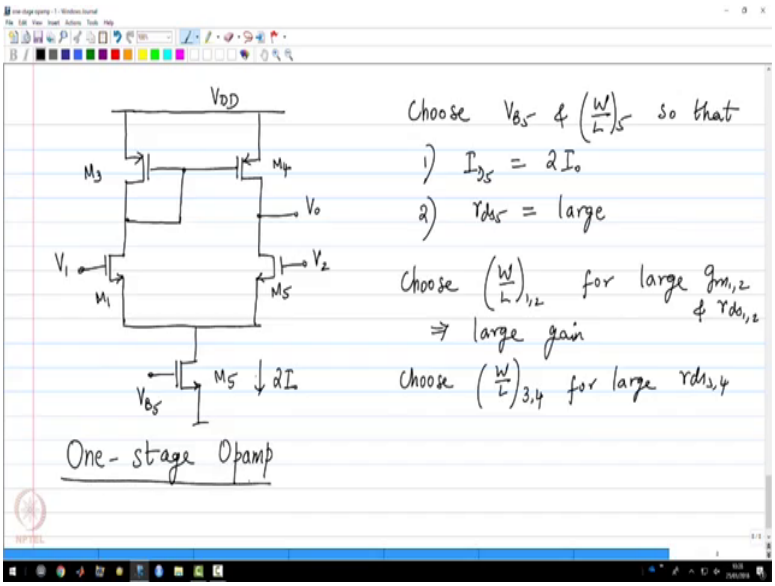

So, we only have one extra addition to make which is that we need to do something about this current source 2Io. So now, as we know a current source can be replaced by a transistor with a bias voltage at it is gait, and this is what we are going to do because we do not want an ideal current source to be hanging out in our circuit. So, we will replace this with a fifth transistor which I will number M5 with some bias voltage connected at it is gate.

The bias voltage and the size of M5 and W over L of 5. So, we need 2 conditions number one the current is 2Io Id5 should be equal to 2Io, and the second condition is that rds5 which is the output resistance of this current source needs to be as large as possible.

So, these are the 2 conditions we are going to use while choosing rds5; while choosing vb5 and W over L 5 the further conditions; there is one more condition that needs to be applied because clearly you have 3 variables vb5, W5 and L5, there are 3 independent variables that

can be chosen, we will study the third condition when in you know when we look at this opamp in a little bit more detail, but these are the 2 conditions as of now.

We will choose W over L of 1 and 2. So, that we get large gm1 2. So, that we get large gain. So, we choose W over 1 2. And how do we choose M3 and M4? So, we choose M3 and M4 for large rds3 4, and just a reminder we also need large rds1 2 for large gain.

So, these are the ways in which we would choose this later on once we study the other aspects of this particular circuit, which is called a one stage opamp. We will be able to choose these in a little bit more detail, but for now we will say that these are the conditions that will be used.