Analog Integrated Circuits
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Lecture – 15

Active Loads

In this lecture, we are going to start looking at a particular type of circuit that is going to try to maximize the gain available from an amplifier.

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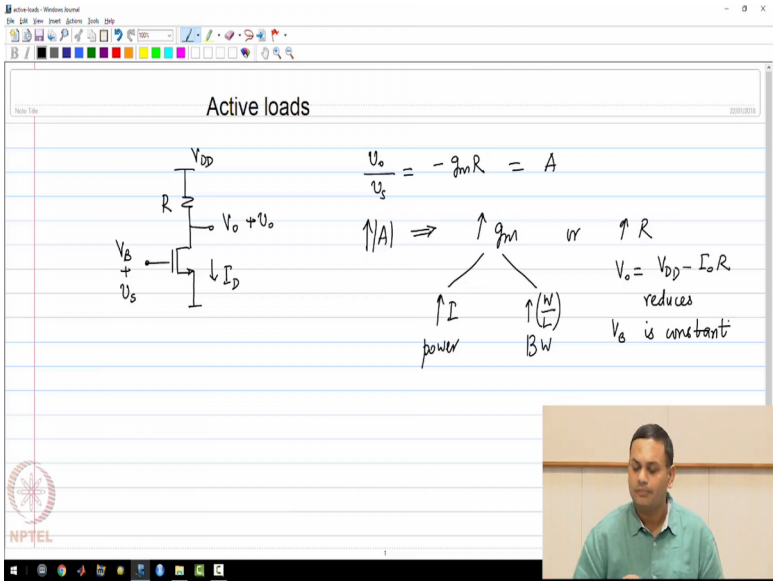

So, so far you would have seen that the common source amplifier gives you the maximum available gain that you can get. So, you will need a bias voltage VB at the gate of the transistor and the small signal is also applied here. The output is of course, taken at the drain. So, maybe I will call this the d c voltage is capital Vo plus the a c voltage is small v o.

So, we know that the gain of this circuit V o by V s is minus g m R. Now suppose I want to get more and more gain from the circuit, I will need to either increase the g m of the circuit or increase the resistance of the circuit.

Now, there is a limit to which you can gain increase the g m, primarily because you do not want to keep increasing the power by increasing the current. So, if I want to increase

g m I need to increase current which means power consumption would increase I do not want to do that.

The other thing that I would need to do is increase the width to length ratio. The otherwise I would need to increase the otherwise, if I wanted to increase g m if I wanted to increase the gain of the circuit. So, this is a I increase A in two ways, I need to increase g m or increase R.

Now, I can increase g m by increasing the current or increasing the w over L of the transistor now all of these has both of these have certain issues.

If I increase I of course, I am increasing the power consumption of the circuit which I do not want to do. If I increase the width and length of width over length of the device I am actually making the device slower because I am increasing the capacitance of the device so the band width gets affected. So, this affects power and this affects band width.

I do not want to affect either of these as much as possible. If I increase R what happens? Suppose I keep the current consumption constant and width and length of the transistor constant if I increase r what I find is that V o the d c value is VDD minus I naught R.

So, if I keep increasing the value of resistance this keep drop reducing. So, the d c voltage at the gate of at the drain of transistor keeps reducing, eventually whereas, the VB stays constant because the current is constant.

So, far you would have seen this type of common source amplifier, and you can write down the various d c voltages in terms of the d c currents and so on.

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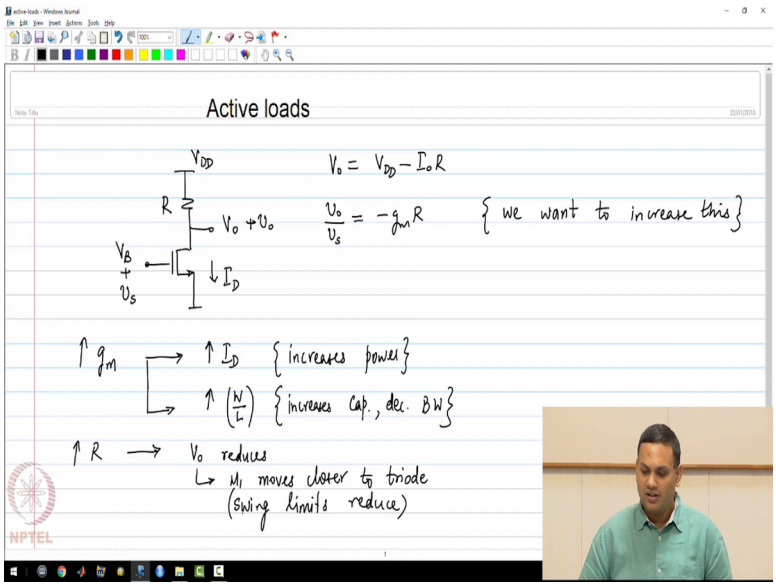

But the voltage that we are interested in is the output d c voltage which is VDD minus I naught R, and we know that for this circuit the small signal gain V o by V s is minus g m R.

Now, let us say that we are trying to increase this gain the magnitude of this gain. So, this is what we are going to try to do.

Now, there are of course, only two ways two parameters that you can touch. So, you can increase the trans-conductance. So, this can be done in two ways, I can increase I D, which I do not want to do which because this will increase power. This increases the d c power consumption which I do not want to do.

The other way I can increase g m is to increase the widths over length ration, and this will increase capacitance and of course, more importantly decreases the band width which is also a problem, I want to keep the band width constant.

And the other way to increase the magnitude of V o by V s is to increase the value of resistance. Now on the phase of it this seems fine, but please note that the output d c voltage reduces linearly with increase in resistance.

In other words the actual implication of this is that M 1 moves closer to the triode region to the triode boundary and therefore, what I am actually giving up is swing limit and this is also a problem.

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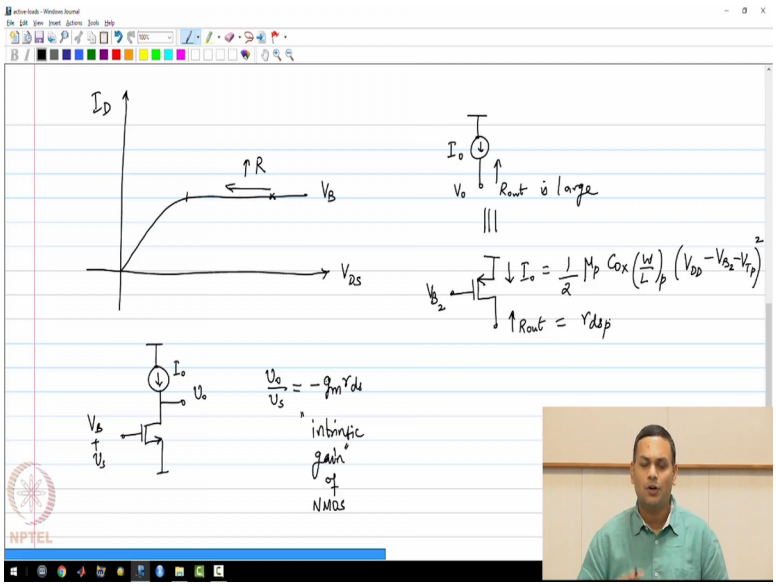

Now, let us show this graphically. So, that we get a better understanding I am going to show this on the plot of ID versus V DS. So, we know that for a particular V B, the ID versus VDS plot looks like this and initially I might have been biased somewhere here VDD minus I naught R d, but now if I increase r for the same VB I will move closer and closer to the triode, let us say this was the triode boundary, I will move closer and closer to the triode boundary which I do not want to do.

Now, it turns out that you need a large value of resistance without changing the bias voltage at the output you may remember from your basic circuit course that if you take an NMOS transistor and bias it using a current source the gain of the circuit. So, V o by V s is nothing, but minus g m r d s and this is the intrinsic gain of NMOS.

So, you may remember that this is the largest gain that you can get from a transistor. So, what we want to achieve is we want to you get a common source amplifier, which has a gain that is as close to this is possible, this of course, does not have strong limitations on output bias point because the current source can have a large range of voltages across it without changing the current.

Now, our job next is going to be to design this is going to be to design this current source, now what we want is we actually want a current source of some value I naught right. So, this was I naught.

Now, please note that the current source is taking some current from VDD and pushing it to ground and; obviously, it has a constant voltage independent of V o, which means that R volt is large. So, these are the characteristics you want from a current source.

So, many of you might realize that a pmos transistor with its source connected to VDD and its drain connected to some VB 1 I will call it VB 1 or VB 2 which is gate connected to VB 2 will have a current I naught that is related to VB 2 in the following manner in this way right.

So, I need to choose VB 2 and w over L of the pmos transistor such that it has a current I naught. What is the output resistance seen at the drain this is of course, the r d s of the pmos which is which can be designed to be very large.

So, now we are going to replace the current source with a pmos transistor, that has biased for a particular current.

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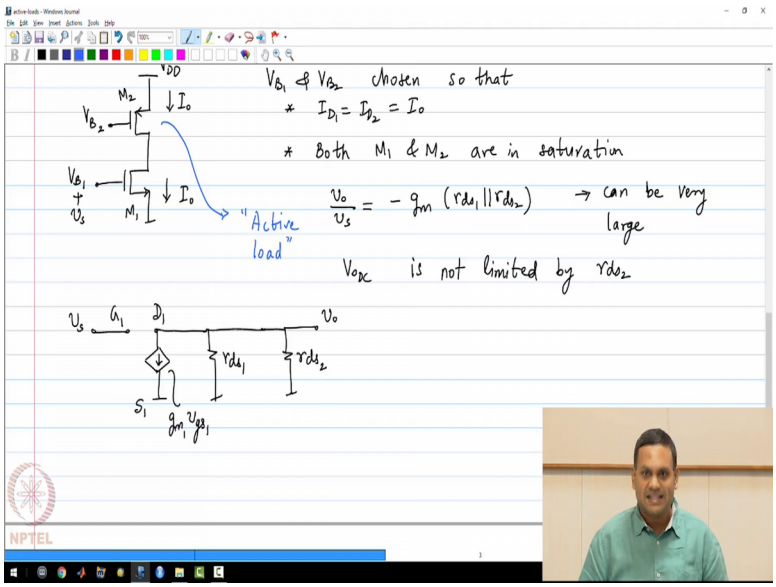

So, this is the amplifier that you have been looking for. So, let us say the NMOS transistor is M 1 and the pmos transistor is M 2 and I am going to say that the NMOS transistor has a bias voltage VB 1 and signal voltage V s applied to the gate, the pmos transistor has some voltage VB 2 at its gate.

Now, you need to apply a voltage VB 1 such that the NMOS transistor has a current I naught, and you need to apply a VB 2 such that the pmos transistor also carries a current I naught.

If you were to draw the small signal equivalent circuit. So, before we draw the small signal equivalent circuit, I want to emphasize again that VB 1 and VB 2 have to be chosen very carefully. So, that the two transistors have the same current I naught and there is one additional condition that is very important I will write it down. Both M 1 and M 2 are in saturation this is a very important condition as you will see. So, you need to choose VB 1 and VB 2 very carefully.

Now, let us draw the small signal equivalent circuit. So, I have a voltage V s which is applied to the gate of M 1, and there is a current source which is g m 1 v g s 1 and r d s 1 of m 1 . So, this is the drain of M 1 this is of course, the source of M 1. Now please note that the drain of M 1 is connected to the drain of M 2 which is also happens to be the output voltage v o.

Now, what happens to the current source of M 2 the voltage control current source clearly the small signal voltage at both the source and the gate of the pmos transistor is 0 and therefore, there will be no signal current generated by the g m portion of the pmos transistor. Now you can write the expression for V o by V s this is nothing, but minus g m into r d s 1 parallel r d s 2. So, now, this can be very very large and. In fact, this is only around half of the intrinsic gain of the transistor, this can be much larger than g m times r because the value of r d s is normally much larger than the value of r.

What about the bias point? Please note that the output voltage V o DC is not limited by r d s of the pmos transistor. So, this is an important distinction compared to the case with the resistor, where the output d c voltage was related to the value of the resistance

In the case of the pmos transistor the output bias voltage can vary over a large range of values without affecting the value of the current or the performance of the pmos transistor.

Now, we can go one step further to complete this whole scenario we can go one step further.

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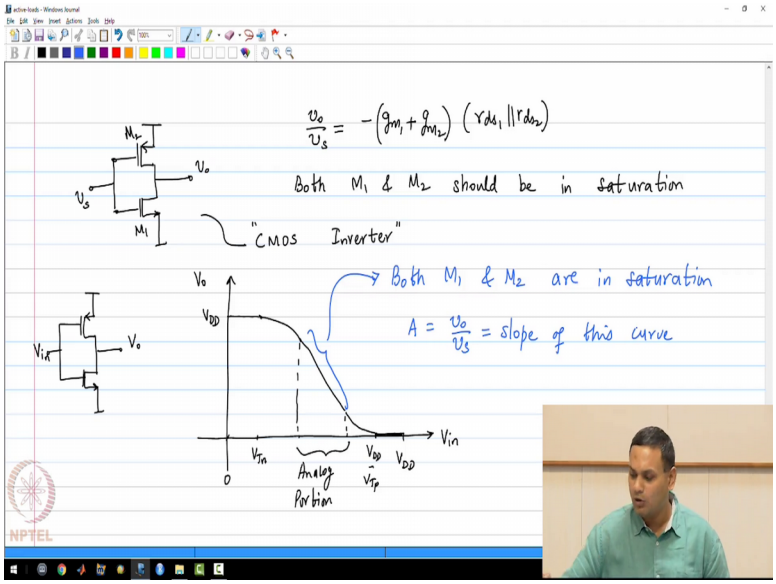

Of course you can also imagine a scenario where you use the pmos transistor for getting some signal gain also. So, what do I mean by that? In the earlier case I was applying V s here and I was connecting the gate of the pmos transistor to small signal ground, but a question can be asked why not connect the gate of the pmos transistor to V s so that you get small signal gain from the pmos transistor also and yes definitely this can be done.

So, let us look at that circuit. So, I am going to this is the circuit that will have V s being applied to the gate of both NMOS and pmos, and I will leave this as a home work, but you can draw the small signal equivalent circuit and show that V o by V s will be minus g m 1 plus gm 2 times r d s 1parallel r d s 2. So, the gain of this circuit will be even higher than the gain of the previous circuit.

Before we proceed further with this circuit I just want to point out that this particular style of using a pmos transistor to get more gain you call this particular pmos transistor by a specific name this pmos transistor is called an active load. So, instead of using a passive resistor a small signal passive resistor which is passive, the pmos transistor actually has small signal gain. So, from a small signal point of view it is active and this is such a way of using the circuit is called an active load.

Now, in this for this particular circuit each transistor acts as an active load for the other transistor. Now an important condition is that both M 1 and M 2 should be in saturation. So, only if both of them are in saturation will you actually get large gain. If any one of

them goes into the triode region you will not get large gain either for this circuit or for the previous circuit.

Those of you who would have taken a course on digital integrated circuits will know that this circuit is actually used in digital design not in a small signal fashion as the cmos inverter.

In those cases you do not apply a small signal voltage at the input and you do not take a small signal voltage at the output. And I encourage all of you to go back and draw the V out versus V in d c characteristics for this circuit. So, if you were to take this circuit and apply a d c voltage V in and look at the output d c voltage V out, if you plot V in versus V out I will give you the curve here I encourage you all to study the circuit and analyze how this happens. So, V in is normally varied between 0 and VDD. So, if you quickly look at the circuit when V in is very small below the threshold voltage of the NMOS transistor, the NMOS transistor is completely cut off and it cannot conduct any current and therefore, the pmos transistor also has to be a nonconductive.

However the source gate voltage for the pmos transistor is very large. So, therefore, the only way this can happen is if the drain source voltage or the source drain voltage of the pmos transistor is almost 0. So, what you will find is that the output voltage till the NMOS transistor turns on, the output voltage will remain at VDD there is no current through the circuit. So, the output voltage cannot change and the drain source voltage for the pmos transistor is clearly 0, it is VDD minus V naught.

After the input voltage crosses v t n you will find that the NMOS can conduct because the V out is very large the NMOS will be in saturation region, but the pmos will be in triode region. Now before I draw the center portion let us look at the other side, if you look at voltages between VDD minus V T p and VDD you will find that the circuit is not conductive because the pmos transistor is off and. So, you will find that the output voltage is 0 and stays 0 because the NMOS transistor is has the drain source voltage of 0.

Eventually the NMOS transistor hits triode and it starts to conduct with the pmos transistor being in saturation. Now there is the center portion where both transistors are in saturation. Now this portion is the analog portion, in this region both M 1 and M 2 are in saturation and this is where you get maximum gain, because please note that the gain a which is V o by V s is nothing, but the slope of this curve it is basically d V o by d v in.

Of course I have shown this is in an exaggerated manner such that the gain is not very high if you actually look at a typical cmos inverter.

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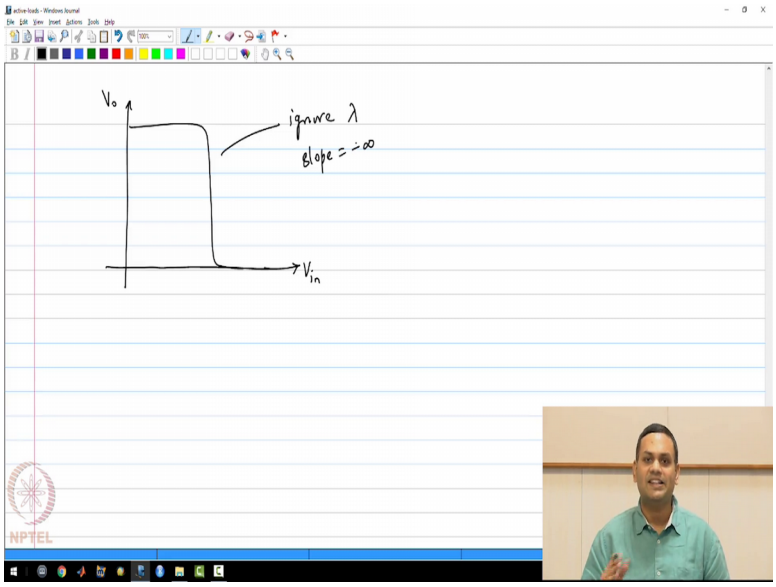

If you look at it a digital I c text books you may actually see a curve that looks more like this. I have exaggerated the curve to show that you know you get large gain you can actually get in an ideal case a cmos inverter should look like this

This is the kind of curve you will see. If you ignore channel length modulation. So, this slope is minus infinity if you ignore lambda slope is minus infinity in other words the gain is infinite clearly because r d s is infinite.

I have shown a case where lambda is very small sorry lambda is very large for the curve shown for an ideal transistor lambda is 0 when you will have r d s equal to infinity. So, there is a range of output and input voltages over which the transistor both transistors are in saturation. This is called the cmos inverter and this can also be used to bias the; this can also be used to get very large gains.