Analog Integrated Circuits
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Lecture - 10
Random Mismatch

In this lecture we will look at the other type of the second type of mismatch called random mismatch. So, we will start first start off with an example device of a Capacitor.

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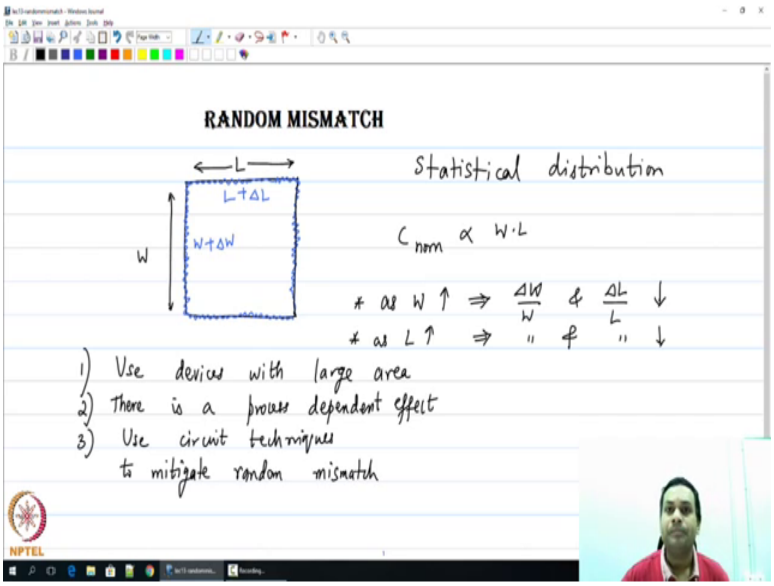

So, let us say that the capacitor has a certain width and length, it is a basically I am showing the top view of the capacitor. So, the this is the top plate of the capacitor, and of course, the capacitance value depends on the area. Now it turns out that if you actually zoom into the edges, what you will find this that the edges at some level are not going to be completely regular. And they are there is going to be some small variation and of course, this variation will be completely random.

so in fact, one of the things that sets apart random mismatch from systematic mismatch is the fact that there is some statistical distribution. So, there is some statistical dependence of this of all or many circuit parameters. Now let us come back to this example because this value now or rather this capacitance now has some variation and it is edge at some microscopic level, you can talk about a nominal value of capacitance which depends on the area of the plate. So, the nominal C norm is proportional to w times L, but the actual value of the capacitance will be slightly different depending on the you know distribution of these defects.

So, therefore, you now need to find a way to figure out how this is going to effective. So, let me say that there is going to be some L plus delta L here. So, I will show that in blue, and this is going to have w plus delta w, and in other words if I take 2 of these devices 2 capacitors may be on the same ic or across ics, I will find that this value of delta w and delta L has a certain distribution. And this particular distribution right will most probably be we will have a Gaussian distribution, but one particular device capacitor may have a particular value of delta w and delta L, if I take a different device I could have a completely different value.

Now, I need to find out a way to minimize this value of delta L n delta w, it turns out if you just do a statistical analysis of this particular structure for example, you could slice this into very small strips either in the vertical direction or the horizontal direction, you will find that the value when you increase the value of the width. In other words let us say you do not do anything to the length and you increase the value of the width it turns out there is some type of averaging effect on both delta w and delta L. So, it turns out that if you do this delta w by w and data L by L both decrease.

Similarly, you will see the same effect if you increase the value of the length of the plate also right. So, this means of course, that if you want to reduce the relative value of delta w and delta L, you have to make sure that the area of the plate is as large as possible. Now in some cases this is; obviously, not easily possible because now you need to find some way to compensate for the increased value of the capacitance. Now I will write the down as maybe 3 points, the first point is if you want to reduce the random mismatch you use devices with large area. Now I have taken the example of a capacitor, but the same is true for a transistor or a resistor or other types of components also.

Now, the second thing I wanted to point out, there is a process dependent effect what do I mean by this? Of course, this is due to microscopic irregularities in the edges. If I do a more finely controlled process or maybe in a different way, I may find that delta L by L and delta w by w is already smaller to begin with right. So, better process can give you a lower a tighter distribution of the random mismatch component and finally, it is possible to use circuit techniques to mitigate mismatch random mismatch.

Now, you will find that these kinds of effects are much more or magnified, when you start looking at a class of circuits called differential circuits. Now when we come to those kind of circuits we will studies the mismatch of the differential circuit. For now we will just take the example of a common source amplifier.

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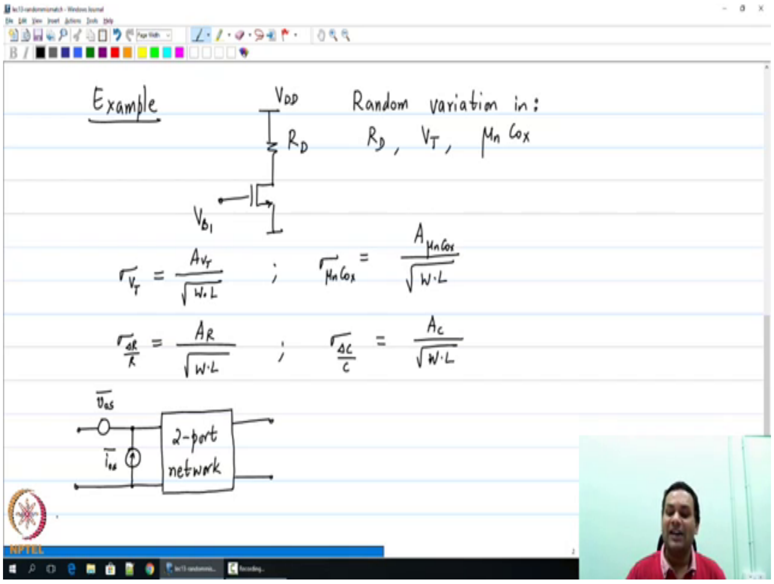

Now, I will assume that the common source amplifier has a resistive load, some resistor R. The input has some bias V B 1, let us say this resistor is R D and the value of the supply voltage is V DD.

Now, what are the parameters that can vary here? The parameters that can vary are the following, if I look simply at low frequencies and I am doing in fact, let us go 1 step further and say I am only going to look at the dc bias point of this circuit. You will find that you could have random variation an R D. So, you can represent that by some delta R D which has a zero mean and some Gaussian distribution, you could have a change in the threshold voltage of the device. So, you might have some delta V T in the device you expect the threshold voltage of let us say 500 millivolts, the actual threshold voltage of the device may actually be 490 millivolts or 510 millivolts.

Apart from this 2, you may also have an error in for example, the capacitances associated with the circuit, but we will not look at that. You may also have an error in the Mu n C ox value. So, let us now right down the expression for the nominal value and the distribution around this, but the point is you will represent those things in terms of certain standard parameters. So, those standard parameters would be the sigma of the V T, all of these remember will have a process dependent parameter now I am going to call that a V T in this case, and it should be noted that they are inversely proportional to the square root of the area, the sigma is inversely proportional to the square root of the area.

Sigma squared will be proportional to the inverse of the area itself. Sigma Mu n Cox again you can represent that in terms of this parameter A Mu n Cox the variation of resistors and capacitors is usually represented in the relative manner. So, remember that the units of a V T, A Mu n Cox etcetera may not be the same. So, this would be AR over root of w times L and finally, if you had a capacitance, this would be A c over root of w times L what is the effect of having mismatch. Before we do the example let us quickly cover that the effect of having a mismatch on any circuit. So, let us represent that by a by 2 port circuit by 2 port network.

It turns out that this effect can be clubbed some very similar to noise, as a combination of 2 sets of variables a series voltage and a shunt current. And I am going to call that some v o s and ios. Now remember that if I take a particular circuit it may have a particular value of v o s and ios, I need to take a large number of circuits depending on the variation of threshold voltages, resistances etcetera I will see a particular value of input referred offsets v o s and i o s.

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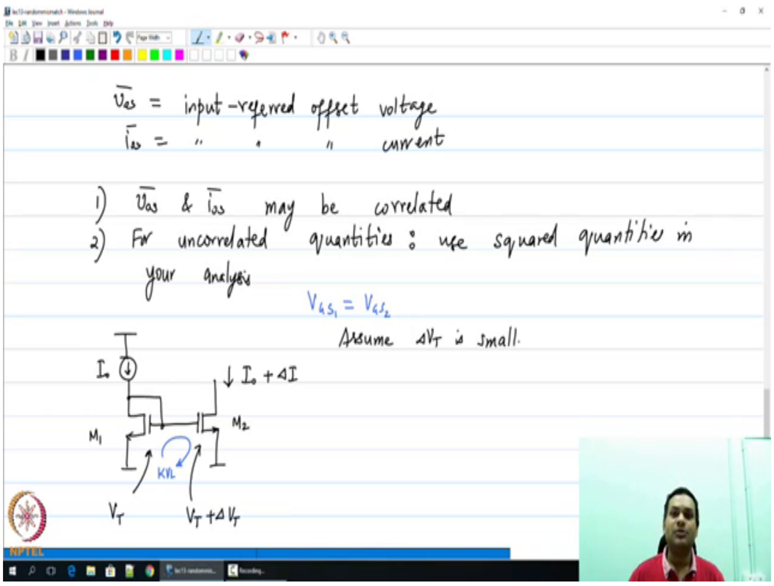

So, v o s is called the input referred offset voltage and ios is the input referred offset current.

Please note that since we are talking about statistical quantities, it is quite possible for v o s and ios to be correlated. I only say may because it is also possible for them to be completely uncorrelated. So, it is possible for them to be wholly or partially correlated. And of course, because we are now dealing with statistical quantities if uncorrelated or rather for uncorrelated quantities, you need to use squared quantities in your analysis.

In other words if 2 quantities if your trying to find the offset voltage due to an random mismatch or a random variation in the resistance, and transistor V T these 2 would move independently and therefore, you need to look at the operate in terms of squared quantities. Now let us go back to an to do our example we will do an example of a current mirror circuit. So, let us say I am going to take current mirror, and analyze it is output current for mismatch. So, this is my input transistor, and ideally my output current should be I naught assuming that M 1 and M 2 are identical.

Now, what I am going to do is, I am going to assume variation in certain parameters, for the purposes of this particular example I am going to assume that there is mismatch only in the threshold voltage of the 2 devices. So, let us say this device has a threshold voltage V T and M 2 has a threshold voltage which is V T plus delta V T. Now the minute I do this the first thing I know is that the both the devices have the same gate source voltages purely by applying KVL around the slope. So, what I know is VGS 1 is the same as VGS 2.

But now because the threshold voltage is a different there will be a mismatch in the output current. So, I will now say that the output current is sum I naught plus delta I, I need to find out the distribution of delta I in terms of the distribution of delta V T. If you do that for this particular circuit the your job is done. So, how do I find out the value of delta I? So, the first thing I can do is assume that this delta V T is small; obviously, nominally the 2 devices better be identical and therefore, any distribution is fairly tightly controlled.

So, I can assume that delta V T is small. So, that is the other assumption I am going to make. Once I do this it should be now pretty straight forward because now delta V T or rather delta V t is going to cause a change in delta I.

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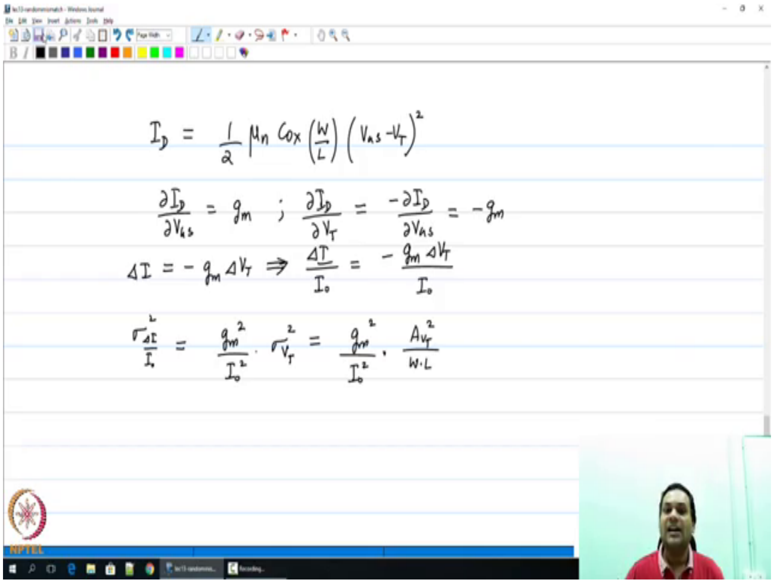

So, maybe if I write down the equations it will be a little bit clearer before I write down the final quantity. So, I know this is the basic expression, I know that dou I D by dou VGS is the transconductance of the Mosfet which is g m, but in this particular case I need to find out dou I D by dou V T.

Now, looking at a equation it should be clear to you that this is the negative of dou I D by dou VGS which is minus g m. Therefore, I can say that for small delta V T the output the change in output current delta I should be equal to minus g m times delta V T. Now what is this negative sign mean for us? What this is telling us is that if M 2 has a larger threshold voltage for the same VGS it is current will be smaller in other words delta I will be negative. If delta V T is positive delta I will be negative and vice versa. So, that is what that negative sign is telling us.

This is well and good, but this is for a particular device for a particular value of delta V T, I now need to find out what the distribution of the delta I is. So, to do that I first need to find out the relative value of this, I need to find out delta I by I naught. So, for a given value of bias current what is the distribution of delta I. This is of course, minus g m delta V T by I naught and. So, let me rearrange this to.

Once I know this what I actually want to find is the distribution. So, I am going to find out sigma squared delta I by I naught. This is actually what I want I want to find out either the standard deviation of the variance, so that I can find out how tight the distribution is of the output current relative to I naught of course. So, this sigma squared delta I by I naught is now going to be g m squared by I naught squared times sigma squared V T. And now what is sigma squared V T this is nothing, but g m squared by I naught squared times AV T squared over w times L.

Now, this is telling us that for a given a V T in a particular process, if you increase the area the relative value if you increase the area of the device, the relative effect on delta I become smaller. For a larger bias current this affect become smaller and so on right. Please also note that you have actually lost the sign the negative sign that you originally had. That is because once you look at the titles of the distribution itself, the actual dependence of delta I on delta V T no longer matters; what you really care about are the mean and variance of the this of the Gaussian distribution itself, at that point you do not care about this negative particular negative sign.