Analog Circuits
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Module - 07
Lecture – 07

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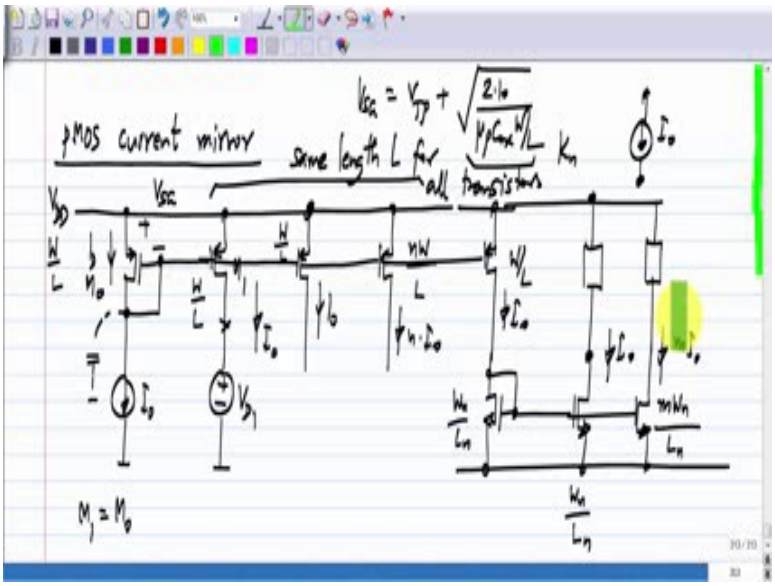

We have seen how to bias both nMOS and pMOS transistors at a given current; and in the nMOS case , we have also seen the current mirror structure which can be used to realise the number of current sources starting from a single current source. Now we will look at a general biasing structure that is commonly used in an integrated circuits to realize number of current sources of both polarities. So, first we look at the pMOS current mirror. And as with nMOS, we start with drain feedback structure where we connect a current source I_o to the drain terminal of the pMOS to sense the difference between I_D and I_o and we know the usual stuff that I_D minus I_o will flow into the capacitor and change the voltage and that voltage can be fed back to the gate of the transistor. It will be in the correct direction to counter the difference between I_D and I_o. In other words, it will be negative in feedback.

And now this V_{SG} , that

$$V_{SG} = V_{TP} + \sqrt[2]{(2*I0)/(\mu p * c ox * (W/L))} \quad ,$$

so this is nothing but the current factor. If you have set of identical transistors, usually you do have them on an integrated circuit, because they are fabricated at the same time and they are very close to each other and they are likely to be at the same temperature. If you replicate this V_{SG} across another identical transistor and I call this M 0 , M_1 and I will write M_1 equal to M 0 to mean that there are matched. Then as long as M_1 is in saturation, let me show something connected to the drain of a M_1 as long as this V_{D1} is such that M_1 is in saturation, this current will be equal to I_o; obviously, here I have ignored the effect of lambda if you do have lambda, the current here will be slightly different from the current there depending on how different the drain voltage here is compared to the drain voltage there.

And it is not just one copy you can make a number of copies again , I draw a line through the gate it simply means that it is connected to this gate and also it comes out here. So, I can have more transistors and more copies of I_o . It does not have to be just I_o. So, let us say all these transistors haves width w and length L then they will have a current I_o and if you makes a transistor of width n*w and the length L it will have current of n*I_o. So, you can also have a multiple of the current that you started with. So, this is how you realise current sources of a variety of values; now one practical constraint which I want elaborate here is that when you do have current mirrors and you want to realize different current values, you change the width, but you do keep the lengths of all transistors are same, because this inverse proportionality to L is not exact.

It does not matter whether it is inversely proportional or has some other complicated dependents. As long as they all have the same L, if you have n*w, you will get n* current. For all transistors, you use same length. Now, we have this currents, but this is still not like a current source whose both terminals are accessible. If both terminal are accessible, if you want to pull current from a node, you connect this; if you want to push current into node you connect that one. Whereas here this terminal is the supply voltage and it is not useful as current source terminal only this terminal is useful. So, with pMOS transistor, you can only push current into the node, but you already know that with nMOS transistor, you can pull currents out of node.

So, if you want both all you have to do is the following. So, let us say you take one of these copies let say this is W/L. So, a current I_o will flow, if it is in saturation region and you realise nMOS current mirror and as many copies of it as you please. So, let say this is W_n/L_n, if you have the same dimensions, and the this transistor is in saturation something has to be

connected here. I will just show it as some load as long as it is in saturation, this current will be I_o and again you have multiple copies also with different dimensions. So, let say the width of this is $M*W_n$, and the length is L_n then this current will be $M*I_o$.

So, you just have a bunch of the pMOS current mirrors and nMOS current mirror. Here I started with pMOS, but you could also other way around. And this structure is very commonly seen in every integrated circuit, because you have a number of components in fact a very large number of components where you need these bias currents and all these bias currents are generated using transistors. And all the circuits that you saw we had the transistors biased at a constant current in our amplifier and control sources because that was a good way of biasing. Now you know where the current sources come from.

So, if you want a current being pushed into some node then you use this type of pMOS current source; if you want current pulled out of some node, you use this type of nMOS current source. So, this is part of every chip and if you start with a single current source I_o, you can get a number of current sources of both polarities, so both pushing and pulling out. If you want to be very precise about it this is called a current source, because it sources current into a node, and nMOS is called a current sink because it sinks current from the node, but it is quite alright to call both of them and current sources. Now how do we get this first one over here, now there are many techniques to do it, and I would not go into all the details one possibility is simply to replace this with a resistor of the correct value, so that you get I_o.

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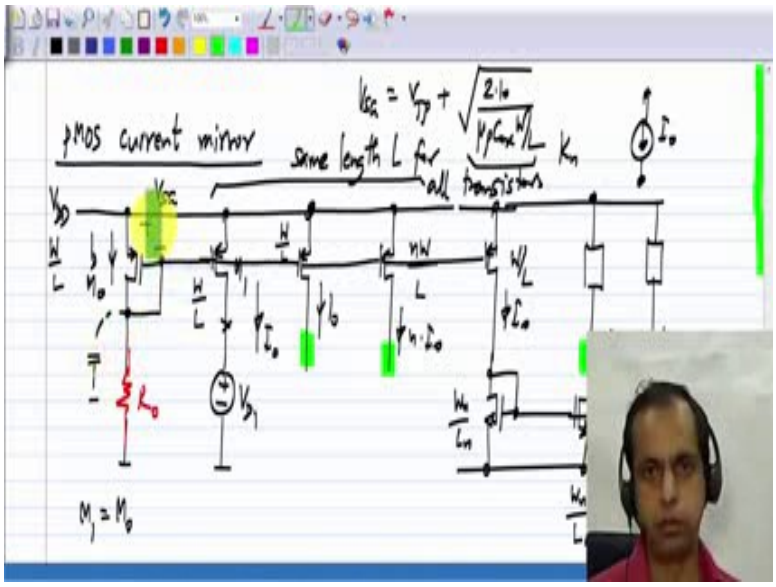

But the problem with that is that as the transistor characteristics change or as supply voltage changes, the voltage across this will change and the current will change even if the resources very precise. Let us assume that the resistor is very precise, it has to be to define the current accurately even then as the voltage across it changes, the current will change that also can be fixed by using a more sophisticated version of this drain feedback biasing.

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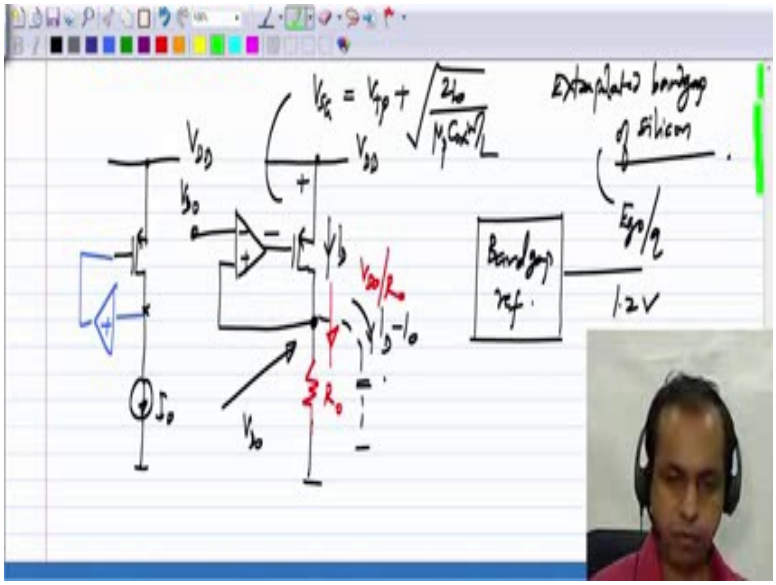

So, how did we do drain feedback biasing, we had our pMOS transistor we connected a current source to the drain. And we saw that the variation required at the gate is in the same direction as the variation that we see at the drain. So, we fed it back directly, but I mentioned before, it does not have to be feedback directly. It could be through any kind of stage, which has a positive incremental gain after introducing the exact topology, you can analyse and make sure that this is in saturation. One such possibility is an op amp which in fact we have used for some other types of constant current biasing So, how do we use an op amp. So, let us say the op amp is here we can feed back to one of the terminals of the op amp and the other terminal can be connected to some fixed voltage let me call it V_{D0}.

Now, we want a positive incremental gate from the drain to the gate of the transistor. So, this should be the plus terminal and this should be the minus terminal. By the way, you can after looking at this topology go back and analyze and see what the signs of the op amp should be and you will see that it should be positive. Sometimes students make a mistake of assuming that wherever the feedback returning to that is the negative terminal, but that is completely

arbitrary, you do not know how many inversion are taking place inside the feedback loop. So, you have to actually break the loop and analyse the sense of feedback and assign the sign correctly.

So, fine now again the same thing happens as before, if the drain current is different from I_o, the differential will flow into the parasitic capacitor I_D - I_o, if the I_D is too small, then current will be pulled out and this voltage will fall down. As this voltage is falls, the gate voltage of the pMOS transistor falls, and therefore, the VSG the source gate voltage will increase , increasing the current. Finally, steady state is reached when $I_D = I_o$ then obviously V_{SG} of the pMOS transistor has to be equal to the threshold voltage plus the required overdrive voltage.

$V_{SG} = V_T$ + Required Overdrive voltage

Now, that is fine that part you know already, but what is so special about this circuit because we have an op amp and let us assume it is an ideal op amp, these two terminals we will be virtually shorted, because of the negative feedback loop. So, this voltage will be exactly equal to V_{D0} and it is independent of the supply voltage and transistor parameters and so on.

So, now, if you replace this current source with the resistor R naught, the current flowing here will be V_{D0} / R_0 . So, if this voltage precisely fixed then this current is also precisely fixed. If the voltage and the resistance are précised, then the current will be précised. Now you can use a precision resistor here because it is just one resistor and with this one resistor, you can get accurate current sources all over the chip. It turns out that a precision voltage source is also available in IC technology, there is circuit I would not go into, it known as a band gap reference and its output voltage turns out to be the extrapolated band gap of silicon at zero kelvin divided by Q that is approximately 1.2 volts.

You know that the band gap of silicon is around 1.1 volts or so, but that is at room temperature. The extra polarity band gap at 0 Kelvin is 1.206 electron volts and output voltage of this will be equal to that voltage, and that will be very precise it is independent of temperature and so on so that is what it is used in a chip to get all these multiple current sources.

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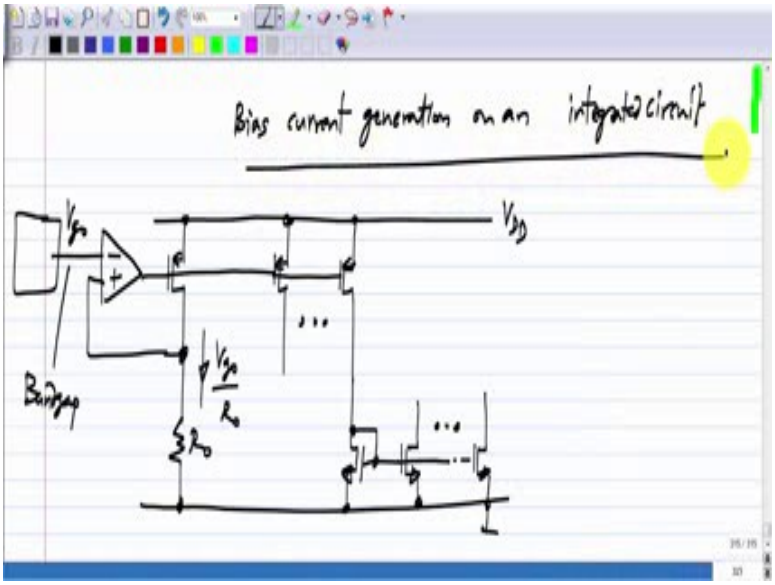

The biasing circuit on a chip could look like this. This is the band gap voltage, and you have one precisely defined resistor its either external to the chip or inside the chip and trim to have the correct value. And then this voltage will be V_{G0} / R_0, and you can replicate the same V_{SG} across many transistors to get copies of the current and you can also get number of current sinks by using nMOS current mirrors. And especially with a MOS transistor, because the gate current is zero there really is no limit to how many transistors you can connect. So, this is how you generate bias currents on a chip.