Analog Circuits
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Module - 07
Lecture – 05

We have seen the pMOS common source amplifier with constant V GS biasing. Now, we look at other ways of biasing a pMOS transistor analogous to what we did with the nMOS transmitter at a given current instead of at a given V GS.

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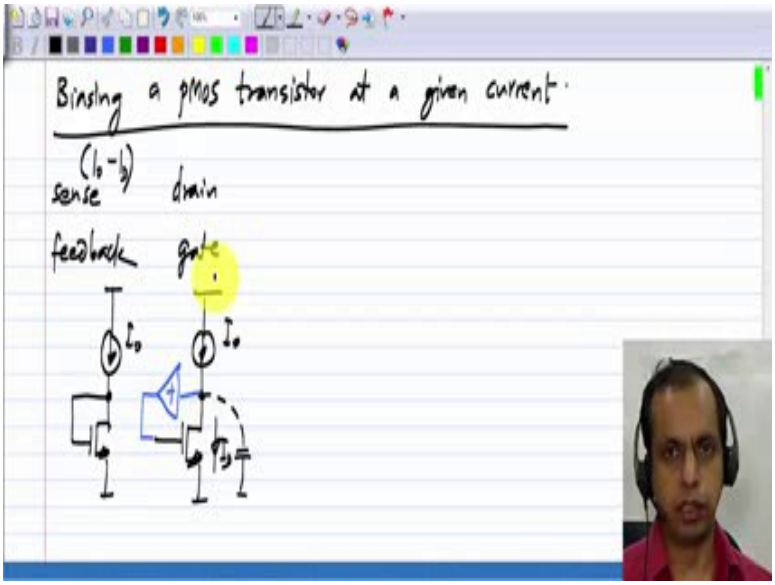

And if you recall with a nMOS we had four variants; we could sense at the drain, when I say sense, sense the difference between the desired current I_o and the actual current I_D at the drain terminal and feedback to the gate and that give us this topology. To sense that, the drain you have to connect the current source I_o over there, so that the difference (I_o - I_D) flows into the parasitic capacitor and changes the drain voltage and to feedback to the gate. You have to complete the feedback through a positive incremental gain that is the gate voltage should increase if the drain voltage increases and the simplest implementation of this is of course, a short circuit where we have this. And we have seen how to realize amplifiers with this.

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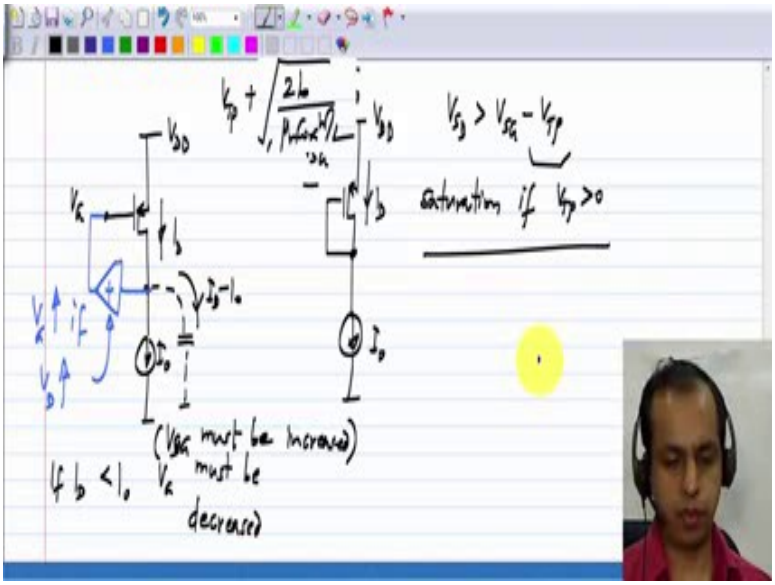

Now if you look at the pMOS of counterpart everything will be the opposite. So, let say I call this V_{DD} that is the source of the transistor which is connected to a fixed voltage. And like I said before because we operate with positive supply voltages, I will call this V_{DD} and the lower rail will be called ground that will be the common reference node of the circuit. And we have to sense the difference at the drain node; this is I_D and this is I_o. So, now the difference I_D - I_o flows into this for parasitic capacitor. If the drain current is smaller than desired then this current will be pulled out and the drain voltage tends to fall down.

Also if the drain current is smaller than desired, if I_D is smaller than I_o the gate voltage V_G must be decreased. This is because the source gate voltage V_{SG} must be increased. So, V_G must be actually reduced. And how do I do that if I_D is smaller than I_o what happens is this voltage goes on decreasing. So, the variation at the drain is exactly in the same direction as the variation we need at the gate. This is exactly the same as in the nMOS case. So, again just like before, we have to the complete the feedback through a positive incremental gain; this means that V G increases if V D increases that is the role of this positive incremental gain.

And the easiest way to do that is by connecting the drain to the gate directly. So, in this case you know that $I_D = I_o$ in steady state; in steady state meaning this voltage is not changing anymore. And if this is V_{DD}, this V_{SG} will be adjusted such that drain current $I_D = I_o$; in other words,

$V_{SG} = V_{TP} + \sqrt[2]{(2 * Io/(\mu n Cox(W/L)))}.$

So, exactly same as what had in case of the nMOS transistor that will be the value of V_{SD}. Now will this transistor be in saturation, for it to be in saturation V_{SD} has to be greater than V_{SG} - V_{TP}. So as long as V_{TP} is positive, which is the most common case then this will be in saturation.

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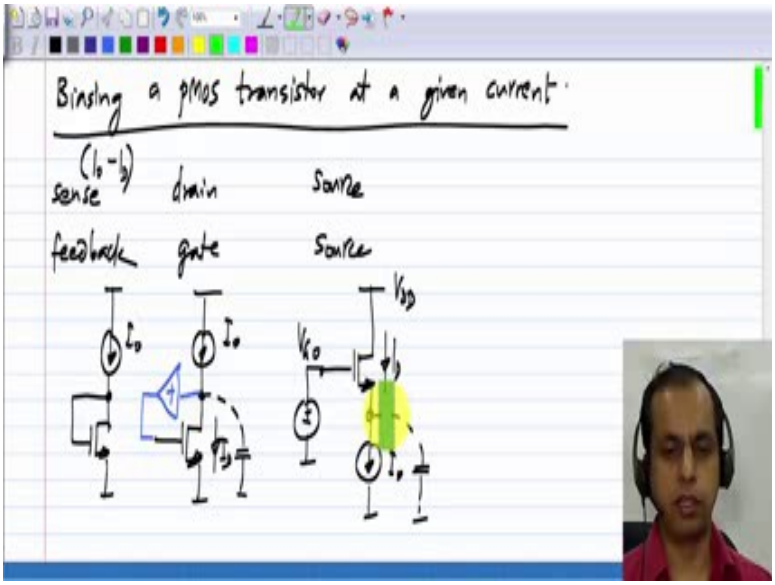

Now, because we have already discussed these things in detail with nMOS, I will go a little quickly through the pMOS alternatives. The second one was to sense at the source terminal and feedback to the source terminal. What did we do in the nMOS case, because we are feeding back to the source, the gate terminal was tied to some fixed voltage V_{G0} , and the drain was not used. So, it was connected to upper rail V_{DD}. To the source we connected a current source I_o and it turned out that we did not have to do anything more because this connection here means that if I_D is more than I_o then current flows through this parasitic capacitor and the voltage increases. And also if I_D is more than I_o we have to reduce the value of V_{GS} , so that I_D is restored to I_o.

To reduce the value of V_{GS} , we have to increase the source voltage, but that is already happening simply because of this connection. And as I mentioned earlier, the source terminal as part of the controlling side and control side of the MOS transistor. So, feedback is implicit

here; there is feedback. If there is a difference between I_D and I_o, the source voltage changes and that will change the drain current; exactly the same thing with pMOS.

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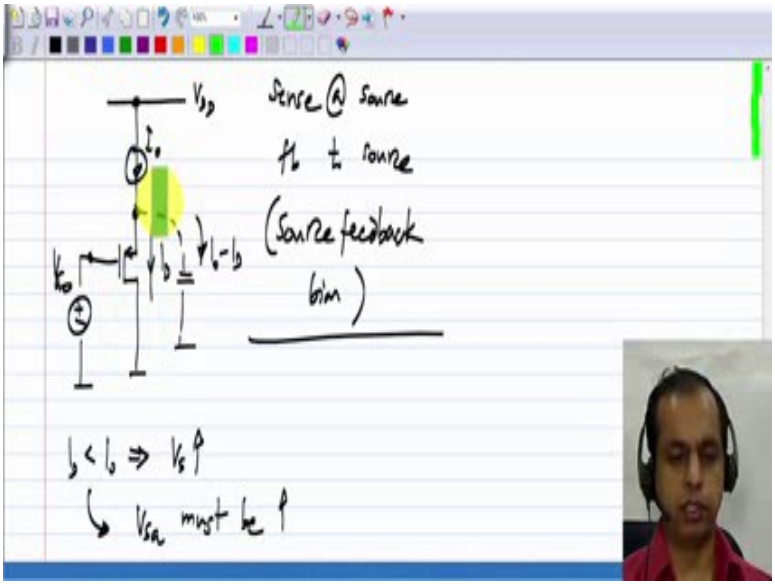

In case of pMOS, the drain terminal is not used at least as far as the operating point picture is concerned. So, we connect it to ground, and the gate is connected to some fixed voltage V_{G0}, usually it is obtained using a resistive divider. And to sense the difference between I_D and I_o, we connect the current source to the source terminal; and any difference I_o - I_D will flow through the parasitic capacitor. So, if $I_D < I_o$, this means that a current get pumped into the parasitic capacitor and the source voltage increases.

Also if $I_D < I_o$, we had to increase V_{SG}. Again you see that nothing more has to be done, because the gate voltage is fixed the source voltage is increasing so that means that the moment you make this connection if I_D is < I_o the source gate voltage V_{SG} will increase. And finally, steady state will be reached that is this voltage will stop moving when I_D equals I_o, so that is all there to it. So, that is source feedback biasing or sense at the source and feedback to the source, source feedback bias with a pMOS transistor. And then using the usual procedure, we can turn this into any kind of amplifier, we have to have this picture for biasing arrangement and the input source and the load must be connected to appropriate places for realizing an amplifier.

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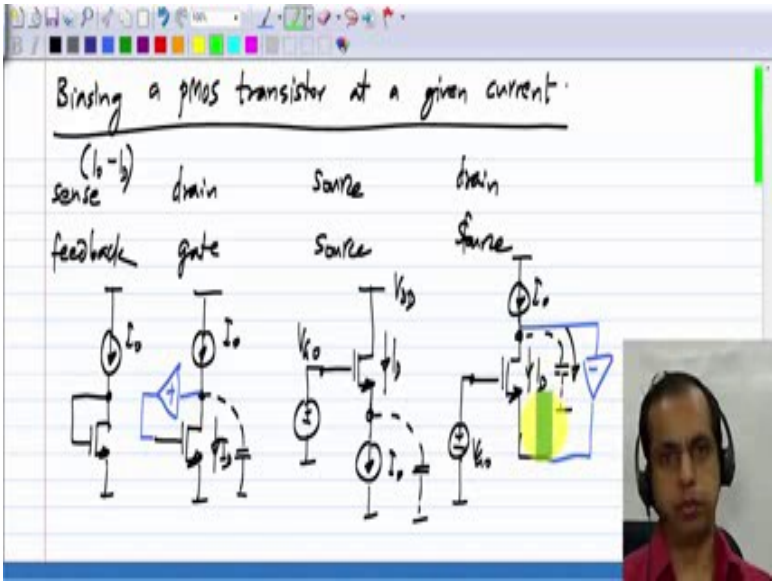

The third alternative was to sense at the drain and feedback to the source. And to sense at the drain, because we are feeding back to the source, the gate is try to a fix potential with V_{G0}. And to sense at the drain, we connect the current source to the drain and any difference I_o - I_D will flow into that parasitic capacitor. And here we know that if I_D is too small, if $I_D < I_o$ then the current will go this way and the drain voltage will increase. The other hand, if $I_D < I_o$, the source voltage must decrease, so that the gate source voltage increases and the current becomes closer to I_o. So, the sense of variation we want at the source is opposite of what we have at the drain. So, we have to complete the feedback through some stage which has an inverting gain which has a negative incremental gain and one of the possibilities is to use as an op-amp.

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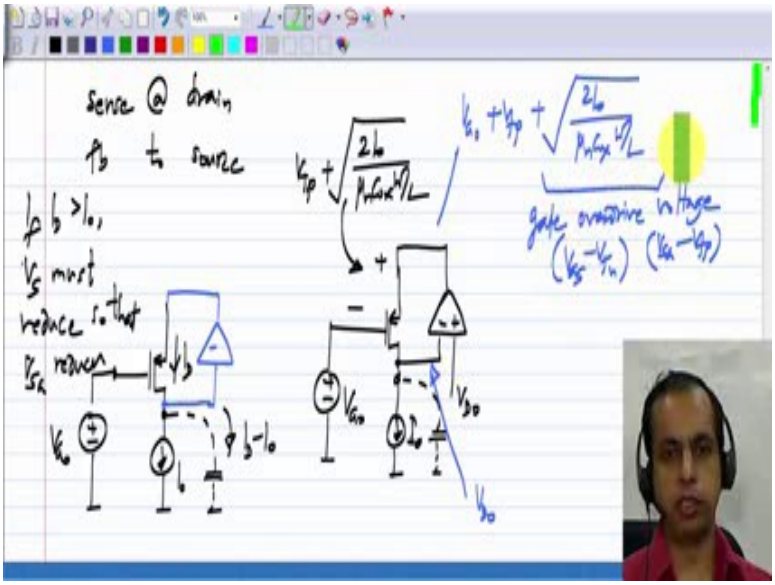

With the pMOS transistor again the gate is tied to some fixed voltage V_{G0} and to sense the difference at the drain this is I_D and this is the I_o. The difference current I_D - I_o flows through the capacitor. If $I_D > I_o$ then this voltage goes on increasing. Now, if I_D is greater than I_o what was happen is that the source voltage must reduce, so that V_{SG} reduces. So the sense of variation, we want at the sources opposite to what we have at the drain exactly as in the nMOS case. So, we need a negative incremental gain between the two that is if the drain voltage increases, the source voltage must reduce.

And a possibility is to use an op amp, there are many things that you can use, but we can use an op amp here. And the gain has to be inverting from the drain to source, so we have minus plus we connect it that way. And if I call V_{D0}, the voltage here will be V_{D0} in steady state, because the op amp I am assuming it is an ideal open, it has a virtual short between its input terminals, so this will be at V_{D0}. And the gate is at V_{D0}, the source gate voltage has to be such that the transistor carries the current I_o it means that the source gate voltages has to be $V_{SG} = V_{TP+} \sqrt[2]{(2*Io/(\mu nCox(W/L)))}$. So, the voltage here at Vs would be the

$$Vs = V_{G0} + V_{TP+} \sqrt[2]{(2*Io/(\mu nCox(W/L)))}.$$

and this part(V_{SG} - V_{TP}) is known as the gate overdrive voltage; basically it is V_{GS} - V_{TN} in case of an nMOS transistor or V_{SG} - V_{TP} in case of the PMOS transistor. It is basically the

amount of excess voltage after turning on the MOS transistor that is present. To turn on the MOS transistor, you need a threshold voltage and beyond that you have this amount and that is called the overdrive.

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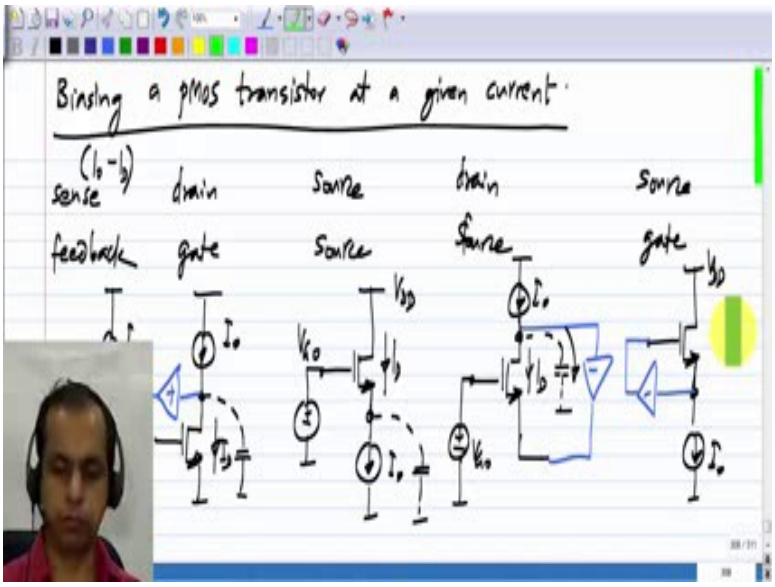

And the last of the possibilities is to sense at the source and feedback to the gate. Again, because now the drain is not in the picture, we just connect it to the supply voltage V_{DD} to sense at the source; we connect a current source I_o. Now, we know that simply by connecting it to the source, we have feedback at the source. In this case, the feedback is not purely to the gate, there will be a feedback to sources as well, but we can provide additional feedback to the gate by completing the feedback through a negative incremental gain. This is because the sense of variation, you need at the gate is opposite to what you have at the source. So, in this case also, I write feedback to the gate there is feedback both the source and the gate, but if this amplifier has reasonably high gain then there is substantial feedback to the gate and lot less feedback to the source.

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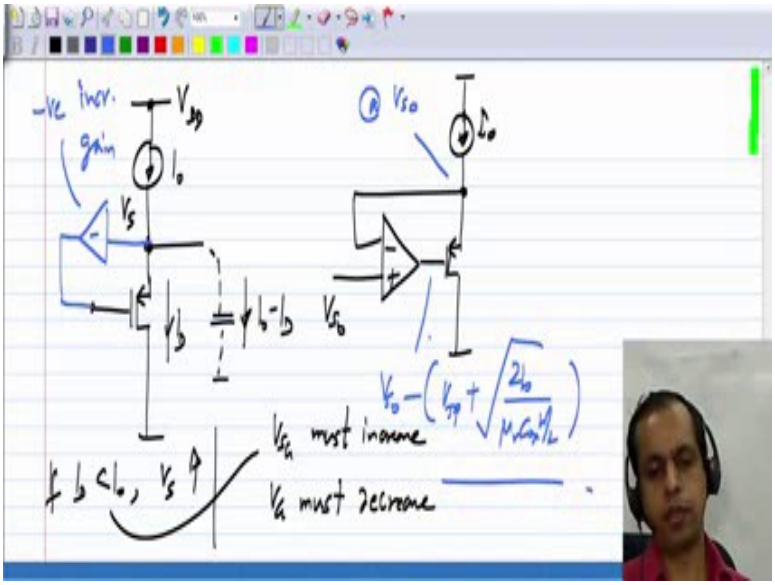

And how do we do this with pMOS same principle. The drain is not used in the operating point picture now. To sense at the source, we connect a current source to the source terminal; this is I_o; this is I_D and I_o - I_D flows that way. So, if $I_D < I_o$, V_S increases; if $I_D < I_o$, V_{SG} must increase. Therefore, V_S must increase or V_G must decrease or both. In this case, V_S does increase, but we also want to have feedback to the gate, so V_G must decrease. So, again the sense of variation, we need at the gate is opposite to what we have at the source. So, we complete the feedback through an inverting stage or something that has a negative incremental gain. So, this really means that the gate voltage reduces if the source voltage increases.

And an example is to use an op-amp, again because we need an inverting structure. We do this, the inverting terminal of the op-amp is here. This is V_{S0} in that , if this is an ideal op-amp, because of virtual sort when it is a negative feedback this voltage will be at V_{S0}. And you can calculate the gate voltage, it will be V_{S0} - V_T + overdrive , that is the last of the variants for biasing a pMOS transistor at a given current. Now, you can take any one of these biasing pictures, and turn it into a common source amplifier or any other kind of amplifier that you wish to have. Now when you already have a working topology with nMOS transistor; you do not have to derive the pMOS topology from scratch. There is a systematic way of converting the nMOS circuit into PMOS that will be the subject of one of the following lessons.