Analog Circuits
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Module - 07
Lecture – 04

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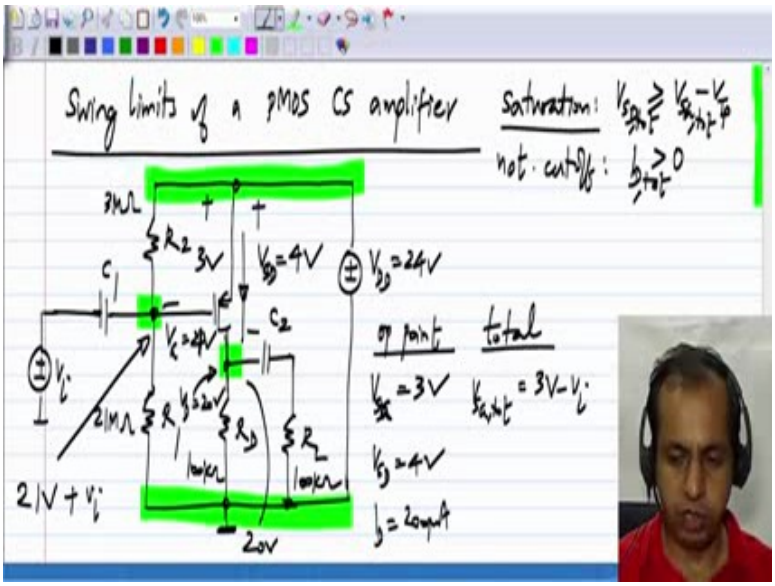

We have seen that a common source amplifier using pMOS transistor has the same small signal picture as that using nMOS transistor and its characteristic also lastly the same. Any differences between these two are only in the parameter values because $\mu_n c_{ox}$ is different from $\mu_p c_{ox}$ and V_{TP} is difference from V_{TN}. You have to use different component values to get the same performance, or if you do use same component values, let say the same load résistance and so on. And the same operating point you will get a different value of gain, but qualitatively there is no difference in the small signal picture.

Now, let us look at large signal characteristic of the amplifier with namely the swing limits. Now, this is the pMOS common source amplifier, and in this case just for simplicity, I will remove this R_s. Although the calculations are exactly the same even with R_s, we always get additional division of this voltage between R_s and ($R_1 \parallel R_2$). I will eliminate that and I also assume that C_1 and C_2 are very large so that we can consider them to be short circuit. So, let say this is 3 MΩ, this is 21 MΩ so that this voltage is 3 volts, and R_D is 100 KΩ and R_L is also 100 KΩ. This is just for the illustration.

Now, this voltage V_{SD} in the quiescent condition is 4 volts. Now why do we have limits on the signal swing, the transistor can go either into triode region or into cut off. So, because of this, the value of input v_i that you can apply to the circuit is limited. So, now, we will investigate this for the pMOS common source amplifiers the condition are exactly same. The condition to remain in saturation is that $V_{SD(total)} \geq (V_{SG(total)} - V_{TP})$. And the condition to avoid cut off, I will say write not cut off is that $I_{D(total)} > 0$ and these refer to not the operating point value, but the total quantities when the signal is applied. So, what we have to do is similar to what we did in case of the nMOS amplifiers, we have to first find the total $V_{SG(total)}$, $V_{SD(total)}$ and $I_{D(total)}$, and apply these conditions.

At the operating point, we have $V_{SG0} = 3$ volts, and $V_{SD0} = 4$ volts. Or if you refer the voltages to ground, the gate voltage is at 21 volts, and drain voltage is that 20 volts. Sometimes for the saturation triode boundary, you specify the condition in terms of $V_{G(total)}$ and $V_{D(total)}$ instead of $V_{GS(total)}$ and $V_{DS(total)}$ that is also possible, so I have written those things down as well. And the current I_D is 200 μA that is of course, flowing downwards. So, you have to keep in this mind that is I_D in a pMOS transistor flowing downwards. Now when the signal v_i is applied, the voltage at this node would be the quiescent voltage which is 21 volts + v_i , because if you did not apply v_i or if you set v_i to 0 , this is a 21 volts with the respect to ground. Remember, when I say voltages at some node, it is with reference to the common ground node of the circuit. So, it is the 21 V + v_i .

Now, this point is 24 volts above the ground because of power supply. So, $V_{SG(total) \text{ is}}$, you can easily see is , if you calculate the total quantity $V_{SG(total)}$ is 24 volts - (the gate voltage) which tells you that it is 3 volts - v_i . Another way to think about it is that if v_i has a positive value then this voltage increases and the source voltage remaining the same. So, the source gate voltage is actually reduces because the gate is going up already you see the crucial different here in case of nMOS common source amplifier this would have been 3 V + v_i or the V_{GS0} + v_i . Now we have a minus in pMOS ($V_{SG(total)} =$ 3 V- v_i) .Now, the voltage here at the drain the quiescent voltage is 20 volts, and what is the incremental voltage at the drain that we get from the small signal picture.

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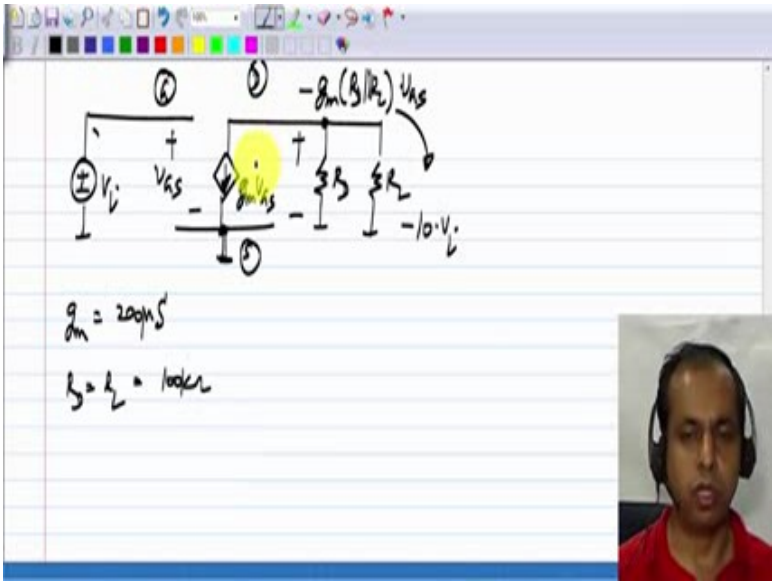

So, we have v_i , and this is the gate, drain and source of the MOS transistor; we have R_D and R_L . So, $v_{GS} = v_i$. So, this is $g_{m*} v_{GS}$, and the drain voltage with respect to ground which is the small signal ground is - g_{m*} ($R_D \parallel R_L$) * v_{GS} . And in this particular case, g_m is 200 µS, and R_D and R_L are 100 KΩ. So, this turns out to be

- 200 µS * (50 KΩ) = - 10 * v_i

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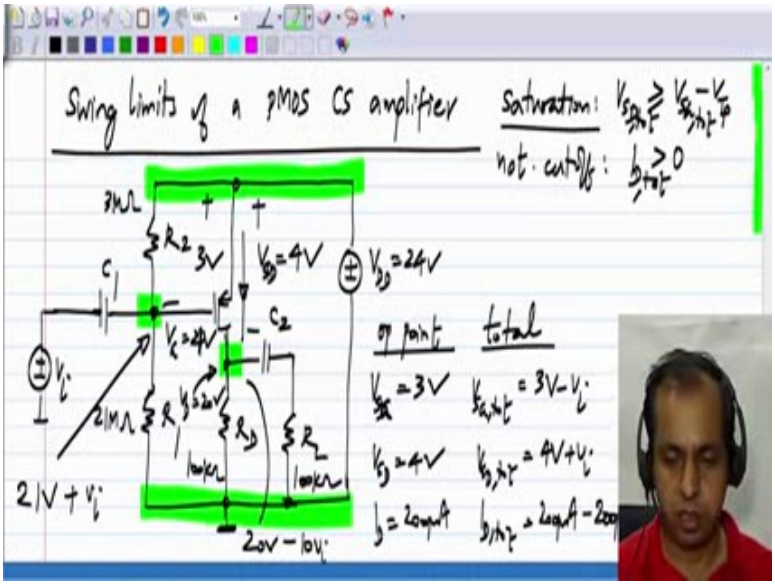

So, the incremental voltage at the drain is - 10 * v_i . So, the incremental voltage here is - 10 * v_i at the drain. So, the total voltage is (20 V - (10 * v_i)). So, $V_{SD(total)}$, you can see is 24 volts

minus this, 24 volts minus this whole quantity. So, $V_{SD(total)}$ is 4 V + 10* v_i . Again you see a reversal of sign and finally, what is the incremental drain current you can see, that is incremental drain current g_m* v_{GS} is going from drain to source, but here the total drain current is going from source to drain, the incremental drain current g_m* v_{GS} going into the drain. So, the incremental current coming out of the drain is - g_m* v_{GS}. So, the total drain current is 200 µA - g_m* v_{GS} or - g_m* v_i because in this case v_i and v_{GS} are the same. It is the 200 µA - 200 µS * v_i. So, you see that the crucial differences lie in these signs.

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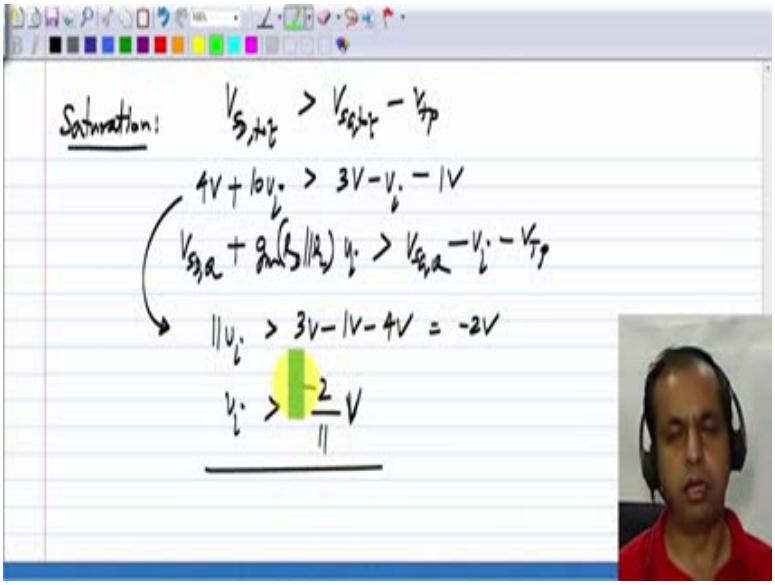

So, what does that mean first let us try to keep the transistor in saturation region. It will be in saturation if $V_{SD(total)} \geq V_{SG(total)} - V_T$, and $V_{SD(total)}$ 4 volts + 10 * v_i . And in general, it will be V_{SD0} at the operating point, I will write it as Q for quiescent point plus gain of the amplifier g_{m*} ($R_D \parallel R_L$) * v_i . And if you have some R_s , you also have to include the division between R_s and ($R_1 \parallel R_2$). This has to greater than $V_{SG(total)}$ which is 3 volts - v_i in this case, and minus the threshold voltage which is 1 V.

$$V_{SD0} + g_m (R_D \parallel R_L)^* v_i > V_{SG0} - v_i - V_{TP}$$

What do I get out of this. So, I get, I take this to the other side I get

$11^* v_i > 3\text{ V} - 1\text{ V} - 4\text{ V} = -2\text{ V}$ or

$v_i > -2/11$ V

Now, if you recall in case of the nMOS common source amplifier, the saturation condition was setting for the upper limit for v_i. Now, it is set the lower limit for v_i. You can see that $v_i >$ - 2 /11 volts.

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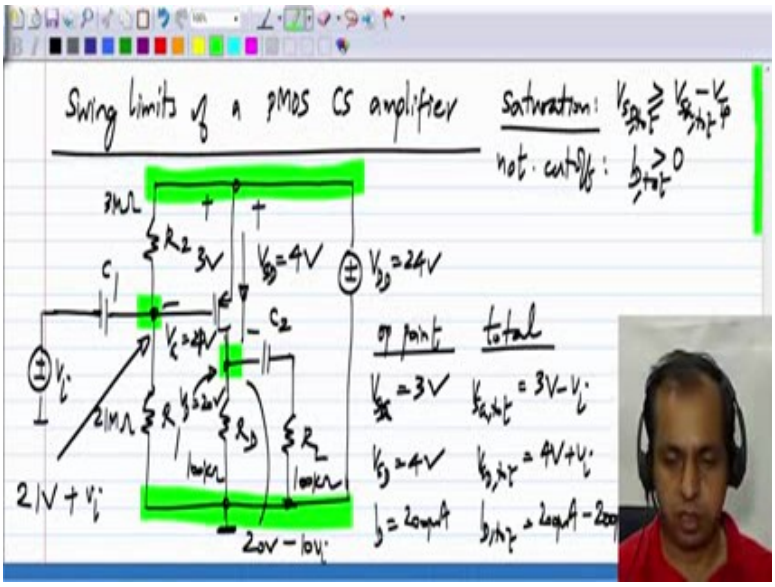

Why does this happen here as v_i becomes smaller, the gate voltage becomes smaller. If the gate voltage become smaller, the source gate voltage becomes bigger and the current through the transistor increases. As the current through the transistor increases, the drain voltage increases because that current is going into parallel combination of R_D and R_L. As the drain voltage increases the gate voltage is falling, the drain voltage is going up, so it is going towards triode region and the triode region saturation boundary actually set the negative limit for the v_i so that the difference. Because the polarities of the currents and voltages are reversed, the swing limits are the opposite in the case of pMOS as compared to nMOS.

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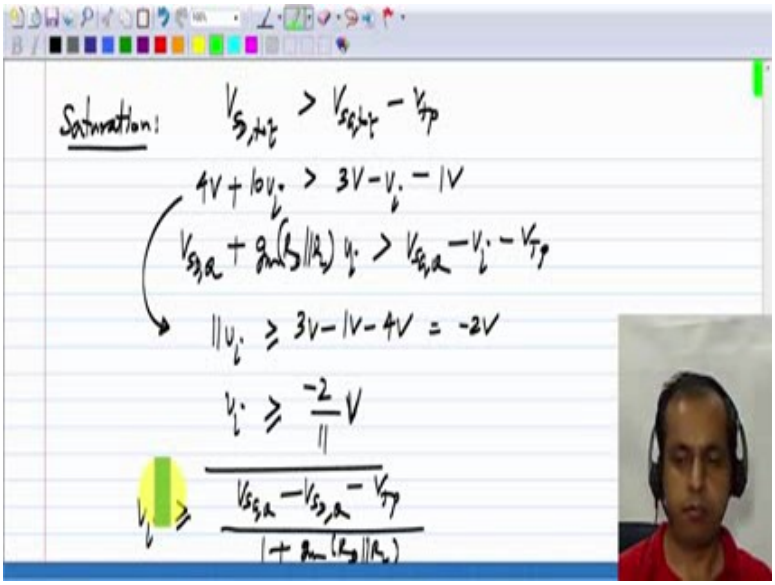

And again I will write it in general terms

$v_i \geq (V_{SG0} - V_{SD0} - V_{TP}) / (1+(g_m (R_D \parallel R_L)))$

I have already explained why these terms come about in case of the nMOS amplifier. We have $1+(g_m)$ in the denominator, because the gate voltage is changing by one unit whereas the drain is changing by gain units. So, the gate drain voltage is changing by 1+ gain units. And if you look at the numerator this difference is the quiescent gate drain voltage or the negative of the quiescent drain gate voltage. So, if the drain is well below the gate then the separation will large and you will get the large swing limit. In case of nMOS, it is the opposite. You want have the drain to be well above the gate voltage so that there is lot of room for it fall; in this case, you have want the drain to be well below the gate voltage so that there is a lot of room for it to rise.

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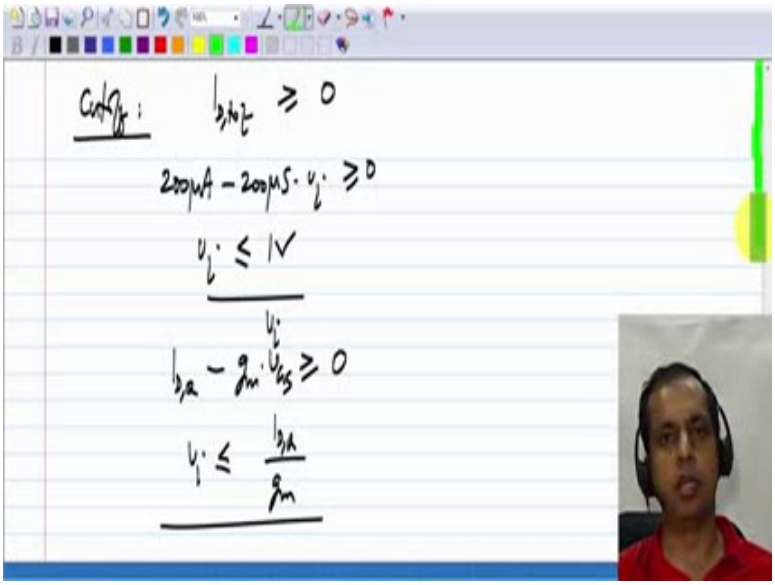

And similarly, if you apply the cut off condition, we want $I_{D(total)} \geq 0$. And again as I explained earlier, we could also have used the condition based on the source gate voltage that is the gate source voltage should be more than threshold voltage, but by convention we use this because we can also use this with bipolar transistor. And what is the total drain current that is the quiescent current $(200\ \mu A - (200\ \mu S * v_i)) \geq 0$. And this tells you that $v_i \leq 1$ V. So, earlier in the case of nMOS common source of amplifier, the cut off condition was imposing the lower limit on v_i, now it imposes in upper limit, because as v_i becomes more and more positive the gate goes up, the source gate voltage falls and the drain current goes on reducing; at some point, it will enter cut off.

In general terms, the total drain current would be the quiescent drain current - $g_m * v_{GS}$ and this has to be greater than or equal to zero. So, and in our case v_{GS} equals v_i .So, this is $g_m * v_i$; $v_i \leq I_{D0} / g_m$. In summary, the small signal picture of nMOS and pMOS common source amplifier is the same and this is true of every other type of amplifiers. If you look at nMOS and pMOS small signal wise there will be same; large signal wise, they will be different. The swing limits in particular are the opposite. If in some circuit saturation imposes on upper limit in the nMOS amplifier; it will impose a lower limit in the pMOS amplifier and similarly for the cut off.