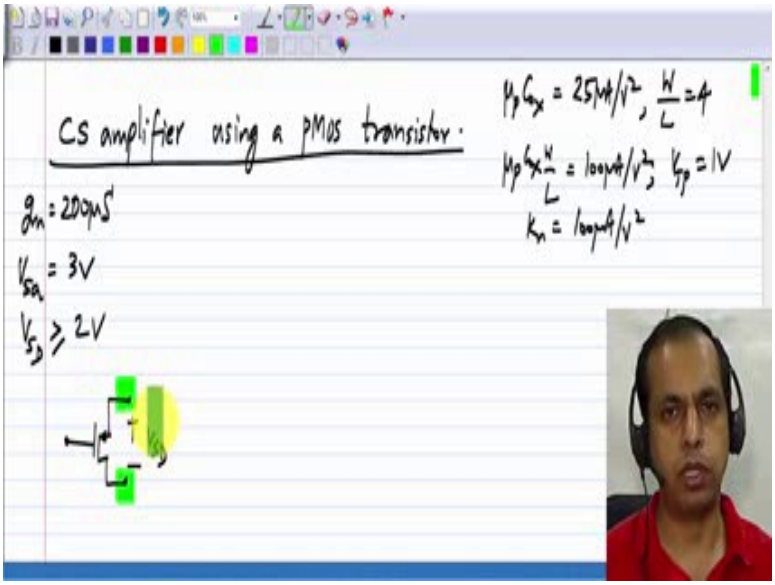
Analog Circuits
Prof. Nagendra Krishnapura
Department of Electrical Engineering
Indian Institute of Technology, Madras

Module - 07
Lecture – 03

(Refer Slide Time: 00:09)

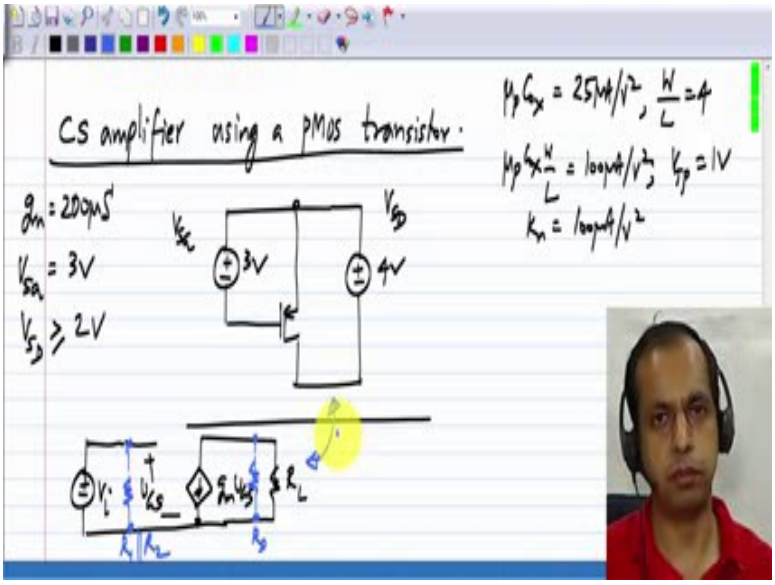


Now, we will try and build a common source amplifier using a pMOS transistor. For illustration, I will use a pMOS transistor, whose $\mu_p c_{ox}$ product is 25 $\mu A/V^2$, and I will choose W/L=4. So, what this does is to have $\mu_p c_{ox}(W/L)$ = 100 $\mu A/V^2$, the same as for the nMOS transistor. So, this is just convenient. So, we can use the results that we already calculated and so on. And I will also assume that the threshold voltage of the pMOS transistor is 1 V , again the same as nMOS transistor, but please do keep in mind that $\mu_p c_{ox}$ $\mu_n c_{ox}$ will be different, and they may not be in this exact ratio 1 : 4.

And also this W/L if you are designing an integrated circuit is variable, you can have W/L which are very small like one or something and you can have 1000 and even 10000 and so on, but we will use these parameters for estimation. Of course, for any other value of W/L , you should able to calculate the parameters quite easily. And I will assume that the g_m , I need is 200 μS . So, if we calculate with this K_n of 100 $\mu A/V^2$ and V_{TP} of 1 volt, you will find that the source gate voltage has to be 3 volts, and the $V_{SD} \geq 2$ V , for it to remain in saturation region.

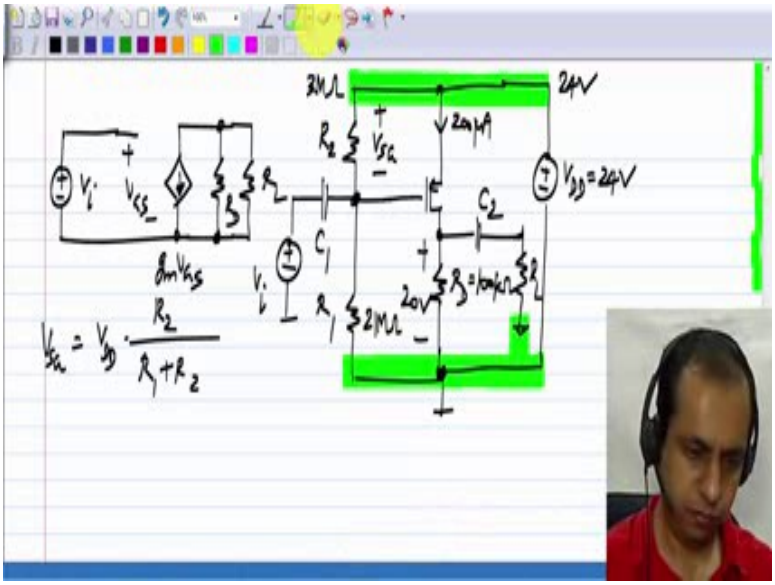
Just as with nMOS, because now voltages will be defined other way do not get confused, just like with nMOS if this voltage, if the difference this and that become very small that is if the difference tends to get squeezed then it goes into triode region. If the difference is large, it will be in saturation region. You can calculate the exact values in case of nMOS, the drain voltage can go below the gate voltage, but not by more than 1 threshold voltage; in case of pMOS, the drain voltage can go above the gate voltage, but not by more than 1 threshold voltage. So, that is what the saturation condition means. First step is to bias it just like with nMOS transistor, we use constant V_{GS0} biasing just for illustration.

(Refer Slide Time: 03:05)



So, we want $V_{SG0} = 3$ volts. So, I will use 3 volts here and we want V_{SD0} of some value. So, let me assume that it is 4 volts. So, this will set up the operating point of the transistor in the saturation region $V_{SD0} = 4$ V and $V_{SG0} = 3$ volts and clearly V_{SD0} is more than $V_{SG0} - V_T$. Now this is how you set up the operating point, and let me imagine that the small signal picture of the common source amplifier is like this. I have some input source v_i and just for illustration initially I will assume that there is no source resistance R_S. So, v_i will be applied as v_{GS} to the MOS transistor we have the control source $g_m * v_{GS}$ and we have the load resistor R_L and just like before from our experience we know that there could be an extra resistance here for the sake of biasing and there could also be an extra resistances here for the sake of biasing. So, now, the question is how to combine the signal picture with this operating point picture.

(Refer Slide Time: 04:50)



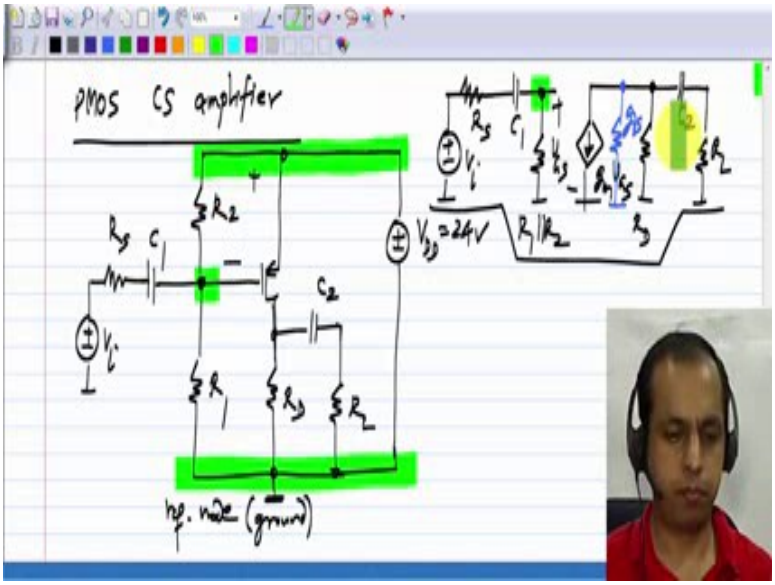
We already gone through this that is why I am going to go little quick, but you should be able to again follow the same logic that we did with the nMOS common source amplifier I will also show R_D because we are going use it anyway this is $g_m * v_{GS}$ and this is v_{GS}, remember R_D is what we use for biasing on the drain side and R_L is the load. We ac couple to the common source amplifier; we already learnt all these things. So, we are going to use them we know them we will use them. So, first let me show this V_{SG0} of 3 volts and pMOS transistor and bias on the drain side will have this R_D. And let me imagine that this is 100 KΩ , and I have to connect the supply voltage I will still call it V_{DD} like that.

Now, we know that V_{SG0} = 3 volts , the drain current of the MOS transistor will be 200 µA and this will be 20 volts and we wanted 4 volts across the MOS transistor. So, this V_{DD} will be 24 volts now , like before I do not want to use two separate DC sources we know what to do this is also generated from the higher source V_{DD} using a voltage divider again because we know all these I will go quickly through this things. So, I will use the voltage divider across the supply and this will provide the source gate voltage bias this is V_{SG0} let me call this R_2 and this R_1 then the voltage V SG is nothing, but $V_{DD}*(R_2/ (R_1+ R_2))$ because this V_{SG0} is across R_2. So, we can adjust the ratio of $R_2/ (R1 + R_2)$ to be the appropriate value. So, that we get 3 volts that is quiet easy for instance I could pick R_1 to be 21 mega ohm and R_2 to be 3 MΩ and I will get 3 volts across this in this circuit the operating point is stabilized we have source drain voltage of 4 volts and source gate voltage of 3 volts and we have to add the input voltage and also connect the load resistance.

How do we add the input to it? It is the usual AC coupling stuff we have v_i and connect the capacitor C_1 to couple it so that if we choose C_1 to be sufficiently large at this point you will get the quiescent gate voltage plus the input voltage, the input voltage will get add it to it. Similarly, the load resistance R_L which have to be ground reference that is one such terminal has to be ground AC couple to the drain of the resistor this is C_2 and so far I have not shown the ground for this supply voltage. In case of the nMOS transistor circuit, we have grounded the source of the MOS transistor that is even in the operating point picture. So, we had this as ground and this is perfectly possible if we call this ground this point will be at -24 volts and there many circuits which do work with negative supply voltages.

But in case of integrated circuits and this MOS circuits in general it is common to use the negative side of this voltage supplier as ground. So, that you think of the circuit as being operated with a positive supply voltage. So, this side is ground and this is quiet common whenever you have a single supplier it is not a rule, but it is quite common. So, when you have a single supply, you think of this bottom rail as ground and up rail as the supply voltage there are exceptions to this sometimes you do have a circuits which run off a negative voltage, but most of the time this is what we do we still called this ground the bottom side and the upper rail will still be at 24 volts. Now as far as incremental picture is concerned this and this are both at ground and this R_L is connected to the common reference note of the circuit which is ground which is on this side.

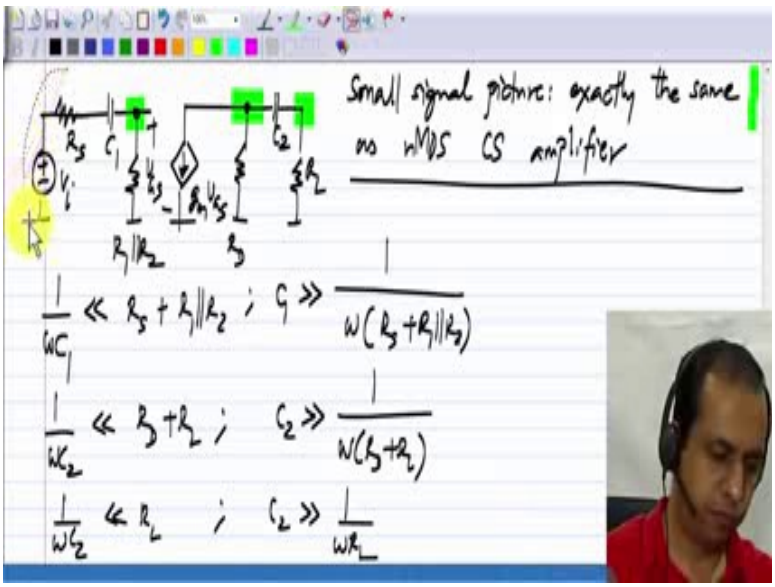
(Refer Slide Time: 10:12)



So, that is the complete pMOS common source amplifier I have v_i and I AC couple it to this point which is the gate and I have AC coupled the load to the drain . The only thing is note that the voltage here is not to source gate voltage the source gate voltage is the voltage between these two points do not get confused by that, but otherwise things are the same the small signal picture of this will be exactly same as before again as I mentioned this side is what is grounded in the nMOS case source of the MOS transistor was the common reference node. And in this case the common reference node is towards the drain side, this is because we preferred operate with positive supply voltages this is the reference node or ground.

Now if you draw the incremental picture of this will have v_i and I will still show C_1 by the way just for simplicity I did not show the internal resistance of this source v_i, but actually I can add it . It is not very difficult to include. So, I will have Rs over there so; that means Rs over here and as far as the MOS transistor is concerned nothing has changed. So, this point is the gate and that is the gate and from gate to ground we have $R_1 \parallel R_2$ because R_1 over here and R_2 there and this point is also incremental ground this is R parallel R_2 then we have $g_m * v_{GS}$ remember the small signal model of the pMOS is exactly same as that of nMOS. When we write it in terms of v_{GS} and then we have R_D from drain to ground, we have C_2 and R_L. This is the incremental picture of the pMOS common source amplifier, and you can see either it is exactly the same as that of the nMOS common source amplifier. And also if the pMOS transistor has non-zero lambda, it will have non-zero output conductance and that is included over there . As usual it just appears in parallel with R_D and R_L.

(Refer Slide Time: 13:47)



So, as far as the small signal picture or the incremental picture is concerned everything is exactly the same between pMOS and nMOS cases, it is the operating point and some other large signal characteristics that will be different . We will see what they are . Now we want C_1 and C_2 to be shorts and we have done this so many times that I will run through it for C_1 to be a short it reactants has to be much smaller than the resistance that appears across it when the source is reduced to zero source is reduced to zero we have R s and this resistance . So, the reactance of the capacitor C_1 , $1/(\omega * C_1) \leq Rs + (R_1 \| R_2)$ or this means that $C_1 \geq 1 / (\omega * Rs + (R_1 \| R_2))$. Now on the output side exactly the same thing holds and I will as usual ignore this g_{ds} , but if it is there it just appears in parallel with R_D .The reactance of this capacitor C_2 has be much smaller than the resistance that appears across it which $R_D + R_L$.

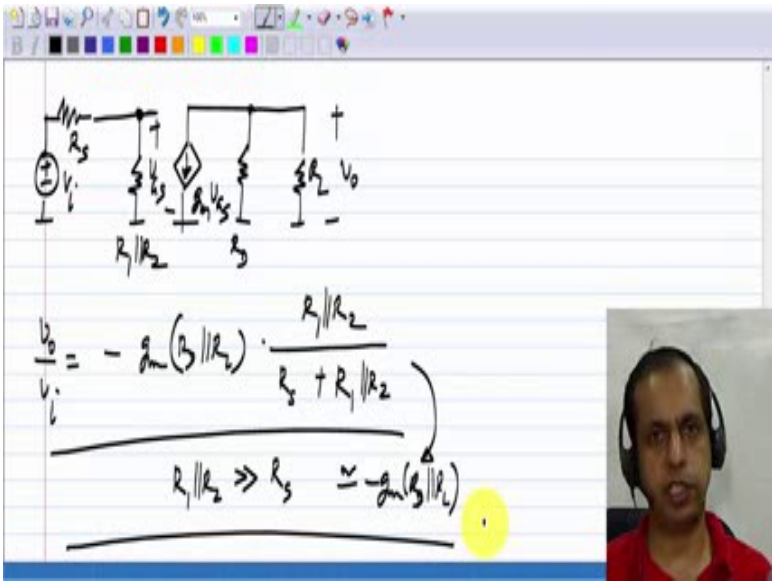
So, $1/(\omega * C_2) \leq (R_D + R_L)$ or $C_2 \geq 1/(\omega * (R_D + R_L))$, but we also discussed earlier that this is the condition that make sure that the voltage at output is same whether you have C_2 or if it is really short circuited this constraints will make sure of that, but sometimes we also need an additional constraint especially if the value of R_D is very high we want this voltage and that voltage to be the same from the discussion on swing limits you know that what limits the swing is the voltage at the drain not the output voltage.

So, if R_D is very large, you could end up in a situation where the voltage swing here is larger than the output voltage. If you have that what it means is that the transistor will going to saturation for a smaller output voltage than you originally thought. So, that is why we want the drain voltage to be same as the output voltage and condition for that is

$1/(\omega * C_2) \leq (R_L)$ or

$C_2 \geq 1/(\omega * (R_L))$

(Refer Slide Time: 16:45)



And once these conditions are satisfied, the capacitor do behave like short circuits that is the picture we have. And we can easily see that V_o / v_i will be - g_m * ($R_D \| R_L$) * ($R_1 \| R_2$) / (R_s + ($R_1 \| R_2$)) .And if you do choose $R_1 \| R_2 >> R_s$ this whole thing will reduce to - g_m * ($R_D \| R_L$) . So, the small signal picture wise nothing is different I just went through it and it is exactly the same as in the nMOS common source amplifier. Now what is really different between pMOS and nMOS stuff, we will see in the following lessons.