Analog Circuits
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Module - 07
Lecture – 02

We have looked at the model of the pMOS transistor, and have seen that it is exactly the same as that of the nMOS transistor, but with current and voltages reversed in polarity. Now what now we will look at the small signal picture of the pMOS transistor.

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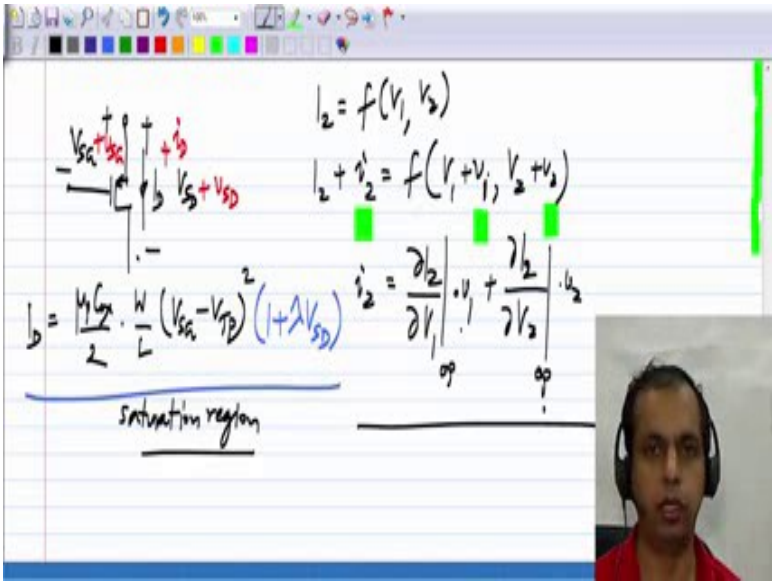

So, just to recap, the large signal characteristic of the pMOS transistor is described in terms of V_{SG} and V_{SD} . And the drain current I_D is written as a function of these two voltages. I will write down only the saturation region equation here $\mu_p c_{ox}/2 * W/ L*(V SG - V_{TP})^2$, this is the model we consider. And just like with nMOS transistor there can be channel length modulation or dependence of the drain current on V_{SD} in the saturation region and that is denoted by an additional factor $1 + \lambda V_{SD}$. I would not draw the graph corresponding to this, but it will be the same that in the nMOS transistor. This of course is only in saturation region.

Now what about the incremental model of the MOS transistor for small increments or the small signal model; if we have any increment of lowercase V SG i.e v_{SG} in this source gate voltage and lowercase V SD i.e v_{SD} in the source drain voltage. There will be a certain current

increment i_D in the drain current. The incremental model or the small signal model describe the relationship between these incremental quantities lower case ID (i_D), V SG (v_{SG}) and V SD (v_{SG}). Now we know that for a general non-linearity if some current, let say I_2 is a function of two voltages V_1 and V_2 then $I_2 + i_2$ (incremental) will of course be the same function of $V_1 + v_1$ (increment in V_1) and $V_2 + v_2$ (incremental V_2). Now what was the relationship between the incremental quantities, we saw that i 2 would be the partial derivative upper case I_2 with respect to V_1 at the operating point times the incremental V_1 (v_1) plus the partial derivative with respect to V_2 at the operating point times the increment V_2 (v_2) and exactly the same thing hold here as well.

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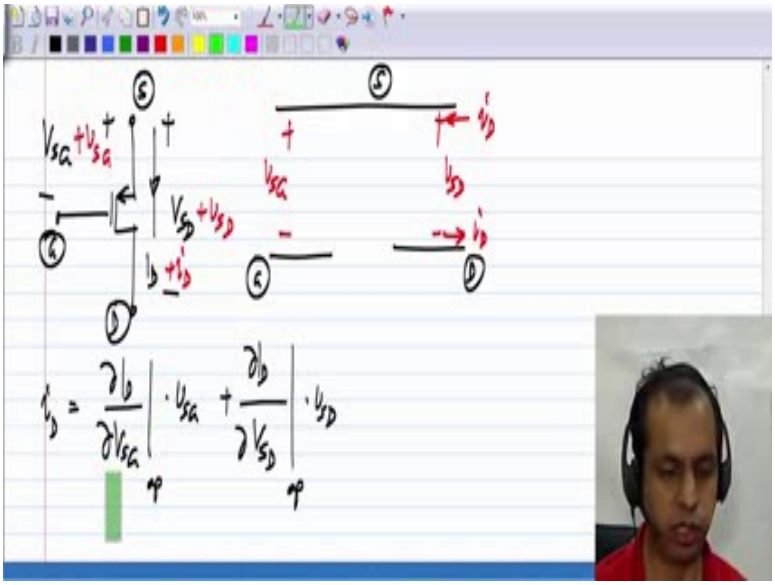

Let us see what that gives us. We have the operating point quantities V_{SG0} and V_{SD0} and I_D let say. And we have the incremental quantities lower case V SG (v_{SG}), lowercase V SD (v_{SD}) and lower case I D (i_D) . Now we want to form an equivalent circuit, which deals with the increments alone. This is source, this is the gate, this is the drain. And similarly, I will draw the source, gate and drain here, and because I G the gate current zero in a pMOS transistor as well. This gate terminal will be an open circuit in the incremental picture. Now this incremental current lowercase I D (i_D) flows from source to drain. This is the incremental currents that is shown in this picture. What is that equal to , it is the partial derivative I_D with respect to V_{SG} at the operating point times the increment V SG (v_{SG}) plus the partial derivative of I_D with respect to V_{SD} again at the operating point times the increment V SD (v_{SD}). So, we

have v_{SG} over here and v_{SD} over there. So, let us consider this quantities one by one, we have a partial derivative with respect to V_{SG} .

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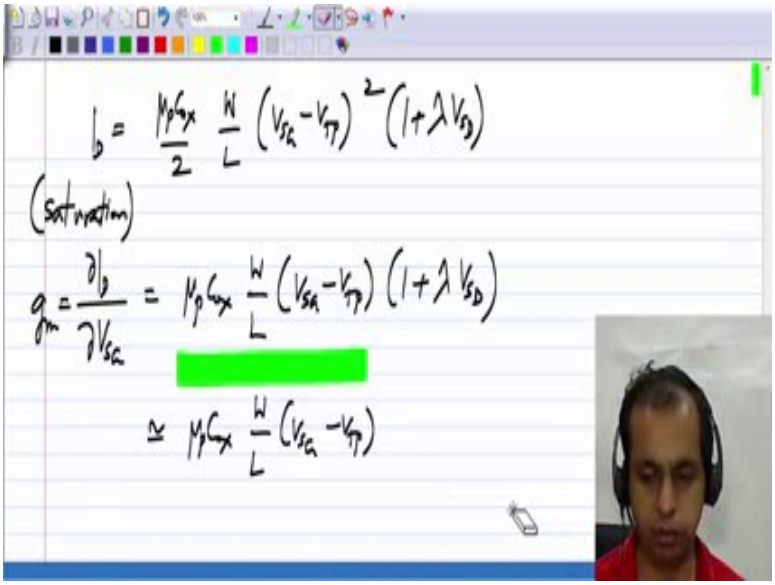

I D again I will do this only in saturation region, but like nMOS you can also evaluated in the triode region and so on.

$(\mu_{pCox}/2) * (W /L)*(V_{SG} -V_{TP})^{2*}(1+ \lambda V_{SD})$.

Partial derivative with respect to V_{SG} is

$(\mu_{pCox}) * (W /L)*(V_{SG} -V_{TP})* (1+ \lambda V_{SD})$

the usual expression of g_m . And many times we even approximated by just this part, because λ is small, this is the same thing that we did for the nMOS case. Usually for most operating point calculations, we just ignore λ, this is nothing but the g_m of the MOS transistor. And you can see that the expression is the same as before except instead of V_{GS} , we have V_{SG} . That is because all polarities in pMOS transistor are reversed and if you have both nMOS and pMOS transistor you could distinguish this saying g_{mp} or using some other extra subscripts.

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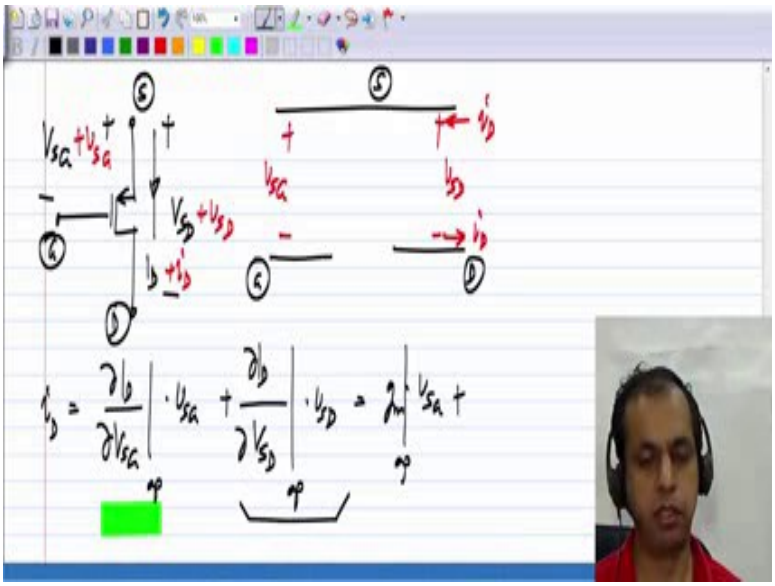

We have the g_m and this simply says that i_D will be $g_m * v_{SG}$ and of course, the g_m is calculated at the operating point that is the value of V_{SG} that you use here, and V_{SD} that use there will be at the operating point . Plus this part here and that again.

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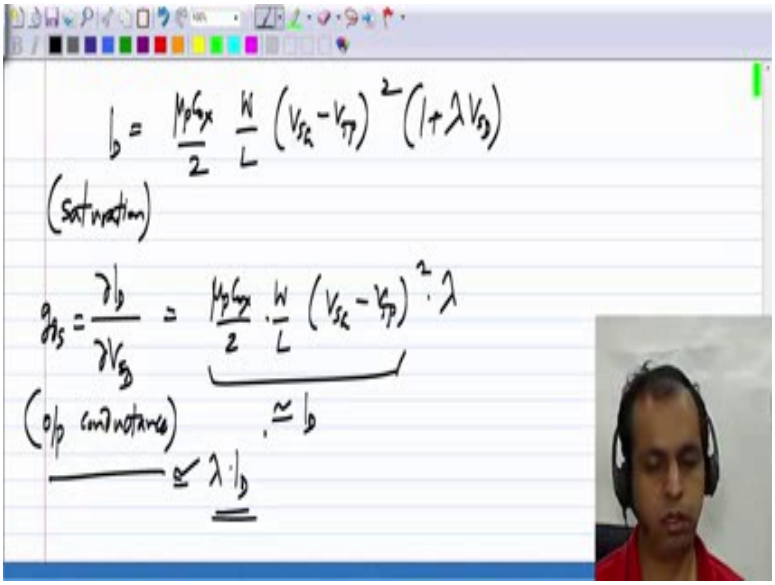

Let me a copy this over there, partial derivative with respect to V_{SD} will be

$(\mu_{nCox}/2) * (W/L) * (V_{SG} - V_{TP})^{2} * (\lambda) = I_{D0} * \lambda$

I_{D0} = operating point current .

So, this is approximately $\lambda * I_{D0}$, and this is the expression that is used most often to calculate this you know what this is, this is output conductance g_{ds} of the MOS transistor.

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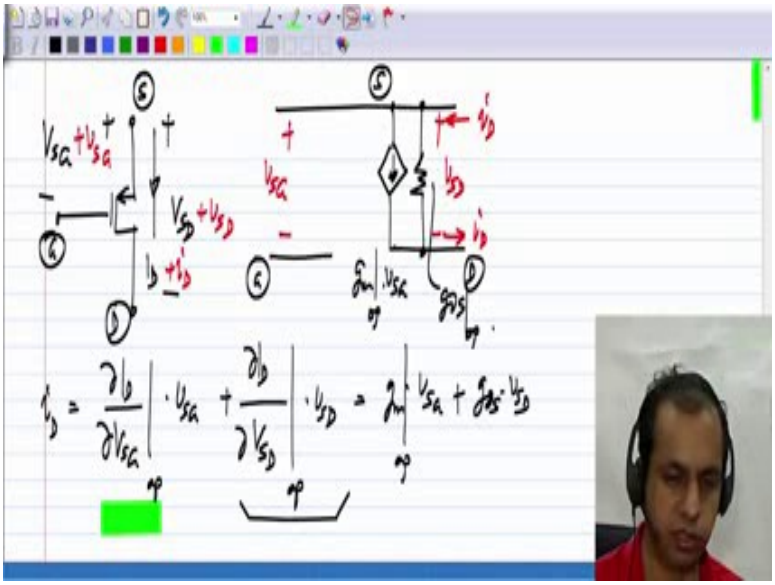

So, the expression comes out very similar to what we had in case of except that instead of v_{GS} and v_{DS} we have we have v_{SG} and v_{SD}. i_D flows from source to drain and it depends on this v_{SG}. So, this term here is represented by a current source which is g_m calculated at the operating point times v_{SG}. And to represent this term , we recognise that i_D flows from source to drain and it is also dependent on the voltage between source and drain. So, it is a conductance this is g_{ds} calculated at operating point it is a conductance whose value is g_{ds} . So, it looks like the incremental picture of the pMOS transistor similar to that of nMOS transistor, but with the polarities reversed but we will make some changes to this that is the following.

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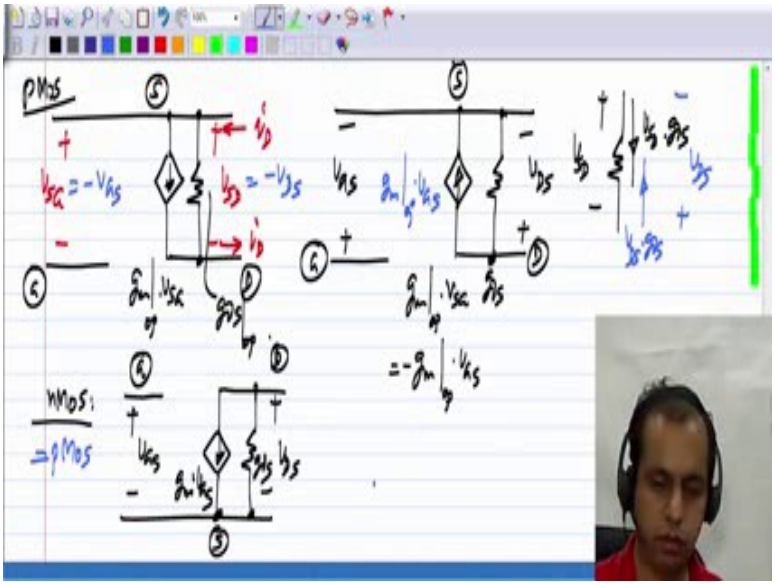

Let me copy this over. Now in case of the nMOS transistor the model was in terms of v_{GS} and v_{DS} , and a picture looks like this. This is a source, this is the gate, this is the drain this is g_{ds} , g_m times v_{GS} , whereas this is the model for the pMOS transistor it is written in terms of v_{SG} and v_{SD} and incremental current source points from source to drains instead from drain to source. Now let us say that we represent this also in terms of v_{GS} and v_{GS} that we can do, because $v_{SG} = - v_{GS}$ and $v_{SD} = - v_{DS}$. If I do that what do I get let me still write the source here, gate there and drain there now I use v_{GS} as the variable instead of v_{SG}.

All I have to do is recognise that this current source is $g_m * v_{SG}$. This current source here is $g_m * v_{SG}$ which of course is $-(g_m * v_{GS})$ because $v_{GS} = - v_{SG}$. And I will also use v_{DS} , as far as the conductance is concerned, the picture remains exactly the same, there is the conductance between drain and source. Obviously, this does not depend on whether you choose v_{SD} or v_{DS} , because if you choose v_{SD} then you will say that $v_{SD} * g_{ds}$ will be flowing in that direction; alternatively if you choose v_{DS} as the variable, which would be in opposite polarity $v_{DS} * g_{ds}$ would be flowing in the direction which is exactly same.

We can see that $v_{SD} * g_{ds}$ going downwards is exactly the same as $v_{ds} * g_{ds}$ flowing upwards . So, there is no change there now this current source here is flowing from source to drain it has a value minus $g_m * v_{GS}$, and I can get rid of minus sign by reversing the direction of the current source I can make it flow from drain to source in which case its value will simply be g_m at the operating point times v_{GS} . why did i do all this , if you do this you will see that the

incremental picture of the pMOS transistor and nMOS transistor exactly the same its not drawn in a weird way, but you see that you have gate source voltage define gate to source the same as here you have this incremental current source going from drain to source the same as here and its value of courses $g_m * v_{GS}$ the same as here and you have a conductance between drain and source. So, incrementally when you express everything in terms of v_{GS} and v_{DS} the pictures of the nMOS and pMOS transistor exactly the same.

So, we will draw the picture this way for the pMOS transistor as well all I did was it started off with v_{SG} and v_{SD} which was the variables originally used to describe the pMOS transistor and I change them to v_{GS} and v_{DS} with that change that you see the incremental picture of pMOS and nMOS are exactly the same. Now this is actually a big advantage because when we try to synthesise the function of any circuit we do it in the small signal domain that is when we realise the control sources and so on. We did it in the incremental domain or small signal domain first and then we added operating point arrangement to it now if the small signal picture of the pMOS and nMOS exactly are same whatever picture we use for on nMOS can be used for pMOS.

So, whatever we derived for incremental picture for all the four control sources or even the common source amplifier can be used as it is, because we will still describe the incremental picture of the pMOS like this , in terms of v_{GS} and v_{DS}, whereas only for the large signal or the operating point picture, we will use V_{SD} and V_{SG} so that is one thing whatever work we did with nMOS transistor can be used with the pMOS transistor. Also when you have circuit with multiple transistors you can first synthesize circuit functionality in the small signal domain without worrying about whether you are going to use nMOS transistor or pMOS transistor in a given place. So, you have many transistors or even a single transistor you can first synthesize the function and later decide which one to use pMOS and nMOS that may be based on some other criterion some measure of convenience or performance. So, all the synthesize of functionality is done in the incremental domain with the model of the MOS transistor which uses v_{GS} and v_{DS} this is so that you can later decide whether to use nMOS or pMOS and this model equally applicable to both.

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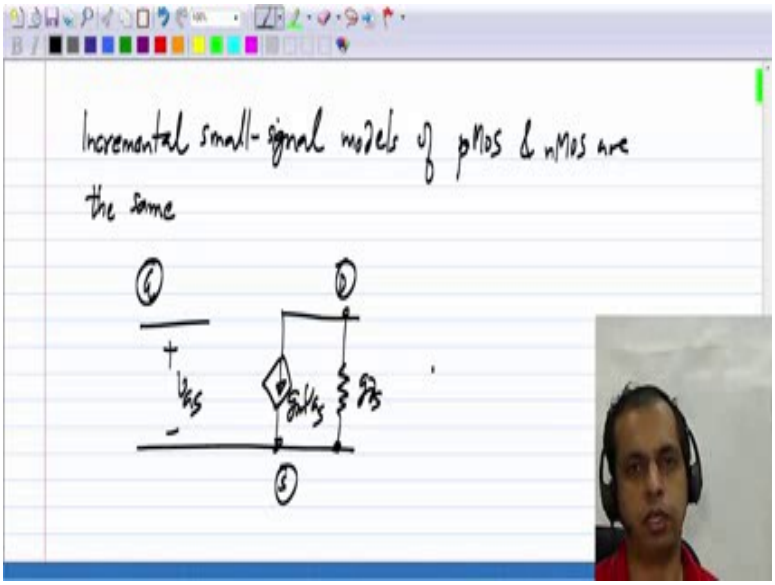

The bottom line is that the incremental small signal models of pMOS and nMOS are the same and it is this and it is usually drawn like this. Atleast whenever possible v_{GS} , g_m* v_{GS} and conductance g_m between drain and source. And in case you are still wondering how nMOS and pMOS came out to have same incremental model.

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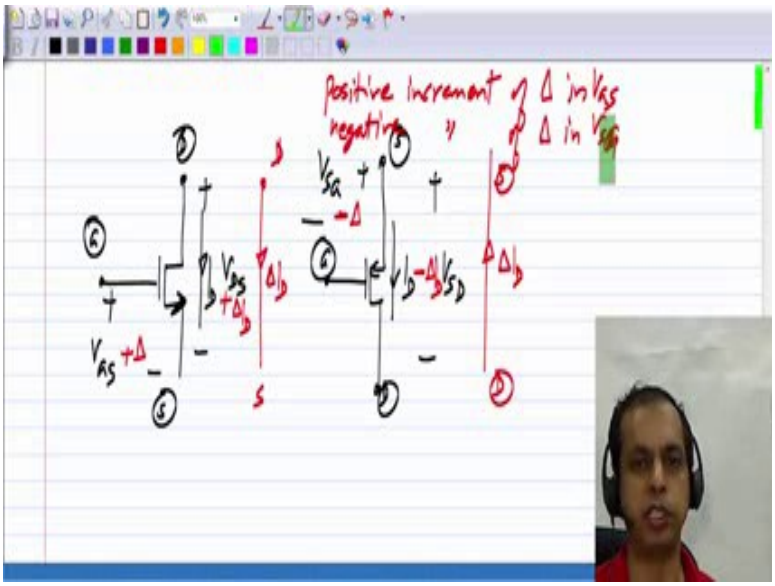

We can also go back to the large signal picture, this is for nMOS and we describe it in terms of V_{GS} and V_{DS} current flows from drain to source , in pMOS on the other hand the current which is defined as flowing from source to drain is described in terms of V_{SG} and V_{SD} now let

me just illustrate this by considering an increment in this voltage V_{GS} (ΔV_{GS}) So, let us say I have positive increment in V_{GS} . So, this means that I_D increases. So, there is a positive increment ΔI_D that is positive increment ΔI_D flowing from drain to source now here I have the voltages V_{SG} and I will consider a positive increment of ΔV_{GS} .So, this obviously, means a negative increment of delta in V_{SG} ($-\Delta V_{SG}$.) So, we have V_{SG} - $-\Delta V_{SG}$ if the value of ΔV_{SG} reduces the current flowing from source to drain reduces and you can equally well think of it as an increment in this direction ΔI_D from drain to source and you can see it is exactly the same. So, a positive increment Δ in V_{GS} will cause increment ΔI_D from drain to source where ΔI_D is positive similarly positive increment of Δ in V_{GS} which is the same as negative increment of delta in V_{SG} will cause the drain current to reduce, but this drain current is flowing from source to drain. So, you can think of it as a positive increment from drain to source. So, incremental pictures are exactly the same for pMOS and nMOS.