Analog Circuits
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Module - 07
Lecture – 01

So far we have learnt how to build amplifiers using MOS transistor. The basic common source amplifier as well as more sophisticated control sources which employ negative feedback. In most of these cases, the preferred way of biasing the MOS transistor was using a current source that is to bias a MOS transistor at a given current rather than at a given gate source voltage. Now, the question is, how do we realise this current sources? Now, we have some idea how to do that, a MOS transistors operating in saturation region itself behaves like a current source.

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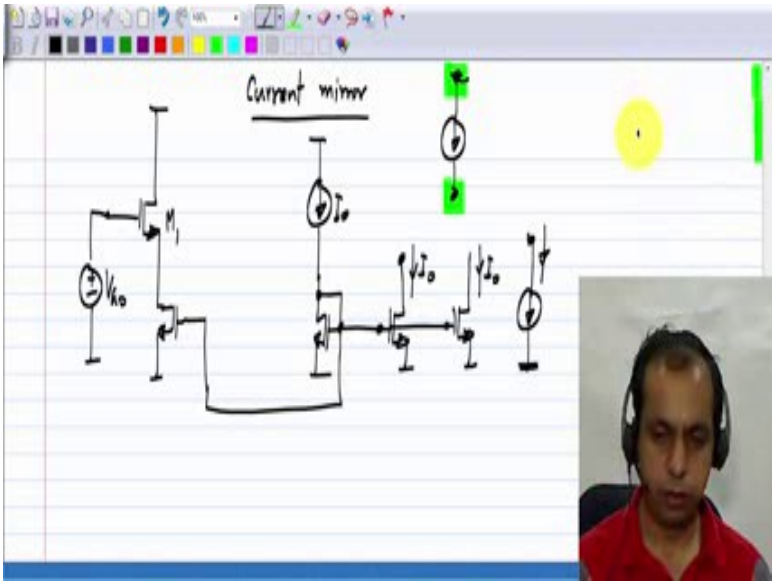

For instance, let say that we had to bias a transistor, I will consider a case of source feedback biasing then we have a current source I_o over here which with negative feedback establishes the current of I_o in the transistor M_1. Now, how do we realise this current source I_o, now there are some ways of realising a single current source that I would not go into, but at least we know the following. We know the current mirror structure that is given a single current source I_o, we can make many, many current sources. .This line here going through the MOS transistor means that it is connected to this gate as well as that gate. So, now we can replicate

this any number of times and all of them will draw a current I_o as long as there in saturation region.

And we can use one such device to bias this instead of this I_o, we can have a MOS transistor. So, assume that these are all identical to each other. .So, this will do the job, but the picture is somewhat incomplete, because with the transistors that we have we can only have currents that are being pulled from a node what I mean is we do not have a current source of this type where both terminals are accessible to us. The current is drawn from this node, current is pushed into this node, but both of these terminals are not accessible to us. What we have is a picture of this type where this side of the current is grounded and we can only have currents which are being pulled from some node.

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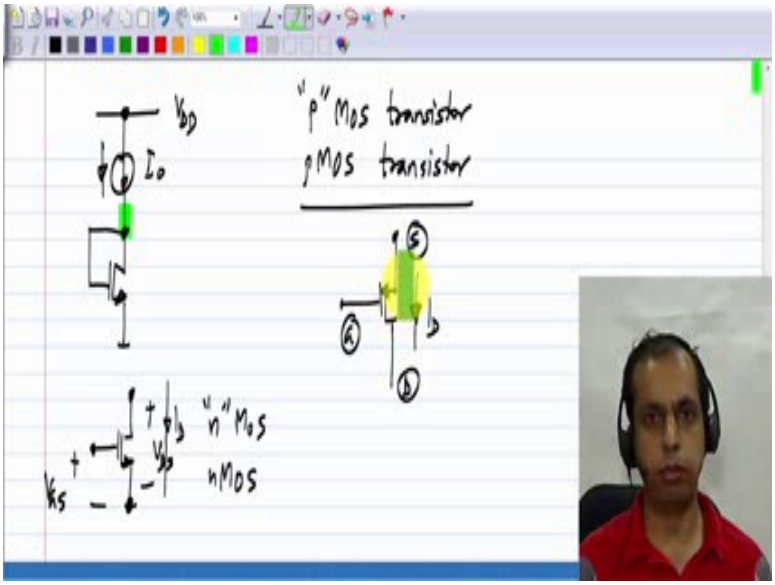

Now if you lo at the case of drain feedback, the circuit was like this where this is the supply voltage V_{DD}, and current has to be pushed into this node. We need a current source in this polarity. How do we make that? And it turns over that with the kind of device that we have we already defined this device this is the nMOS transistor, I used to call it MOS transistor, but it turns out the device that we have been considering so far which operates with V_{GS} and V_{DS} greater than zero. And current flowing from drain to source this is known as n type MOS transistor or usually it is called the nMOS transistor. Now with this type of transistor with nMOS of transistor, it is hard to solve this problem, it may be done, but it is quite difficult,

but thanks to technology we also have the complementary type of transistor which is the p type of MOS transistor and it is called pMOS transistor.

Now, it turns at the desires exactly complementary characteristics to the nMOS transistor denoted by the symbol and I will draw the source on top and the drain at the bottom. I will explain later why this is the usual convention and in this case the current flows from source to drain I will still call it I_D. But in case of the nMOS transistor it flows from the drain to source whereas here it flows from source to drain and this is the complementary type and this is quite useful for making current sources of this type. But of course, it is not only useful for making current sources you can also make amplifiers using that. So, what will do is now to discuss the characteristics of this pMOS transistor and see how to set up the operating point and how to realise amplifiers using the pMOS transistor.

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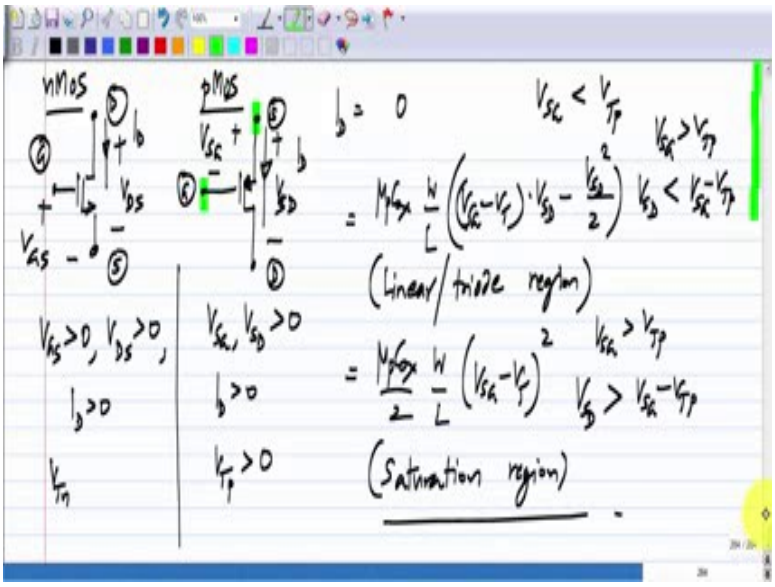

Just for the sake of comparison, I will put down the nMOS transistor here; this is the drain, gate and source. And we choose the gate source voltage and the drain source voltage as a independent variables while describing the current I_D the drain current that flows from drain to source, and the gate current is zero, this is the nMOS transistor. And in case of the pMOS transistor, again I have drawn the source on top, and drain at the bottom, and gate is here. We choose the source gate voltage V_{SG} , and the source drain voltage V_{SD} as the independent variables and that describes the drain current I_D, which flows from drain to source.

So, you should know this convention. So, that when you write down current equations it comes out in the correct direction. The nMOS transistor we said operates with V_{GS} greater than zero and V_{DS} greater than zero that is V_{GS} and V_{DS} are positive in this polarity and I_D is also greater than zero that is always flows from drain to source and exactly the same as true here that is a V_{SG} and V_{SD} are greater than zero so that is in this polarity we will have positive voltages. In fact, that is why it is usual convention to draw the pMOS transistor with the source on top in drain at the bottom. Typically, we like to draw circuits in a way that as we go up the page, the voltage levels increase. Now, this cannot be followed for every circuit especially when you have ac voltages alternating quantities, but at least for operating point as you go from bottom to top, the voltages will increase.

So, in case of a p MOS transistor, the sources is at a higher voltage than the drain, so you draw the source on top and drain at the bottom. And I_D of course, is positive in this direction I will continue to call it drain current, but this current flows from source to drain. If you look at text book, there is a variety of choices for describing the pMOS and nMOS of course, always described with V_{GS} and V_{DS} and so on. Now, sometimes the pMOS stuff equations are written with V_{GS} with V_{GS} being negative and so on, but we will stick to this. So, that all that quantities are come out be positive as long as you know which direction it is in it should be fine.

Now, the model of the pMOS transistor is exactly same as the model of the nMOS transistor the values of the parameters maybe different that is all. So, in this I_D in a p MOS transistor is zero, .if V_{SG} is less than V_t . And again this is technology dependent, but for the most frequently used the flavour of the transistor the threshold voltage is also greater than zero. And sometimes to distinguish between the threshold voltage of n and pMOS will start writing V_{TP} for the pMOS of threshold and V_{TN} and for the nMOS threshold; they could be different from each other in a given process on the same chip.. So, it is a similar phenomenal like in the nMOS, the voltage difference between these two V_{SG} has to be greater than some amount for the transistor to turn on; otherwise, the current will be zero.

And it is equal to $\mu_{pCox}*(W/L)*((V_{SG} - V_{TP)*} V_{SD} - V_{SD}^2 / 2)$. and this holds when the transistor is on that is V_{SG} is greater than V_{tp}, and the source drain voltage is less than V_{SG} minus V_{tp}.. And this of course corresponds to the linear or triode region. You can say that again the equations are exactly the same instant of V_{GS} we have V_{SG} and instead of V_{DS} we have V_{SD} that is all. .And also this parameter denoted μ_{pCox}, the mobility of holes are the p-type carriers

is different from the mobility μ_n of electrons, so this we use a different symbols for, μ_{pCox} is different from μ_{nCox}, it is usually smaller than μ_{nCox}..

Also in other region, we have $(\mu_{pCox}/2)\ (W/L)\ (V_{SG} - V_{tp})^2$ this holds when the transistors on of course,

$V_{SG} \geq V_{tp}$ and

$V_{SD} \geq (\ V_{SG} - V_{TP}\ )$

that is , this corresponds to the saturation region. So, you can see that the model looks exactly the same only thing is the parameter is different V_{TP} could be different from V_{TN} and μ_{pCox} also will be different from μ_{nCox} usually substantially smaller. So, if you draw the characteristics of pMOS transistor, they will lo similar to the nMOS transistor

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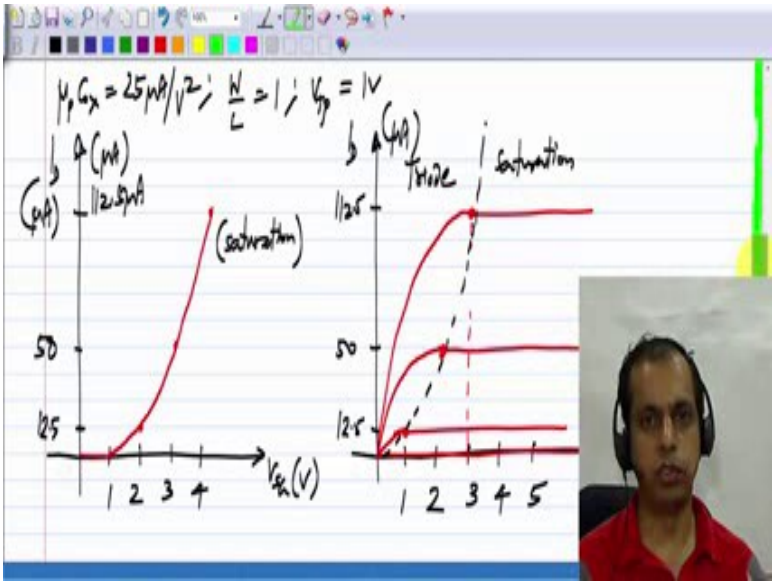

Let me take some typical parameters that may say μ_{pCox} is 25 $\mu A/volt^2$ again (W/L)=1. And I will take the pMOS threshold voltage V_{TP} to be one volt as well. And with this I can draw I_D vs V_{SG} of the PMOS transistor in saturation region. This is in volts and this is in µA . You are already familiar with what the shape los like; up to the threshold voltage, it will be off and there will be no current; and after that it increases as the square of V_{SD} or (V_{SD} - V_T) to be precise. And you can work this out for yourself that at V_{SG} equals 2 volts will have 12.5 µA of current; and at V_{SG} = 3 volts it will be 50 µA . So, we will be here and there and there. So, at V_{SG} = 4 V will have one 12.5 µA. So, in saturation region it will be like that.

Let us write that saturation region is assumed here there also draw I_D vs V_{DS} and the shape of course, similar to what you see with an nMOS transistor when $V_{SG} \leq V_{TP}$ we have no current in the transistor. When $V_{SG} = 2$ V , the current rises up to 12.5 μA and stays there in saturation region. When $V_{SG} = 3$ V, it rises up to 50 μA and stays that way in saturation region. And when $V_{SG} = 4$ V , it goes that way. And this is the boundary between triode and saturation regions. So, essentially everything is exactly the same in a pMOS transistor as an nMOS transistor. The polarities of voltages are reversed and the current is also reversed; it flows from source to drain instead of from drain to source. And the other thing that is different is the value of the parameters themselves, this μ_{pCox} and V_{TP} could be different from μ_{nCox} and V_{TN}. So, those things are there, but qualitatively the behaviour of the pMOS transistor is exactly the same as that of the nMOS transistor except for reverse polarities. This also means that every circuit that we realised using nMOS transistor can also be realised using the pMOS transistor, so that will be the subject of subsequent lessons.