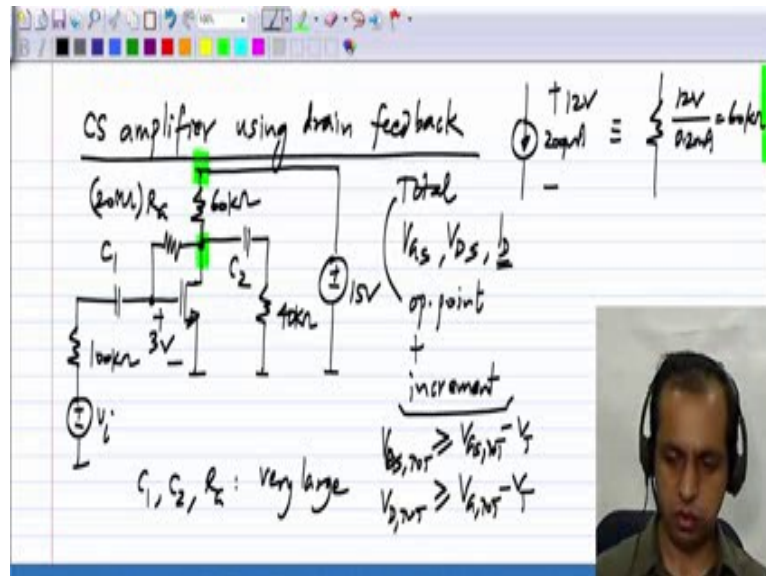


Analog Circuits
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Module - 06

Lecture – 14

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To illustrate calculation of swing limits, we will now study these swing limits of common source amplifier with a different biasing arrangement that is using drain feedback. Now the common source amplifier using drain feedback looks like this. We have the input source which is ac coupled to the gate of the transistor, and there is a current source which biases the drain and there is feedback to the gate using a very large resistor R_G and of course, there is the load. And for illustration, let me assume that the supply voltage is 15 volts; this C_1 , C_2 , R_G are all very large; very large meaning and they are very large, you can make certain approximations essentially that R_G almost behaves like an open circuit and C_1 and C_2 behave like short circuits.

Now, if this is 100 k Ω , and let us say $R_G = 20$ M Ω or so, this constraint is easily satisfied; C_1 and C_2 , I would not evaluate, but we have done it many times and you know how to do that. And let me say that the load resistance is 40 k Ω . Just to make it more interesting, and also to illustrate a point which will come later I will assume that this current source here this 200 μ A

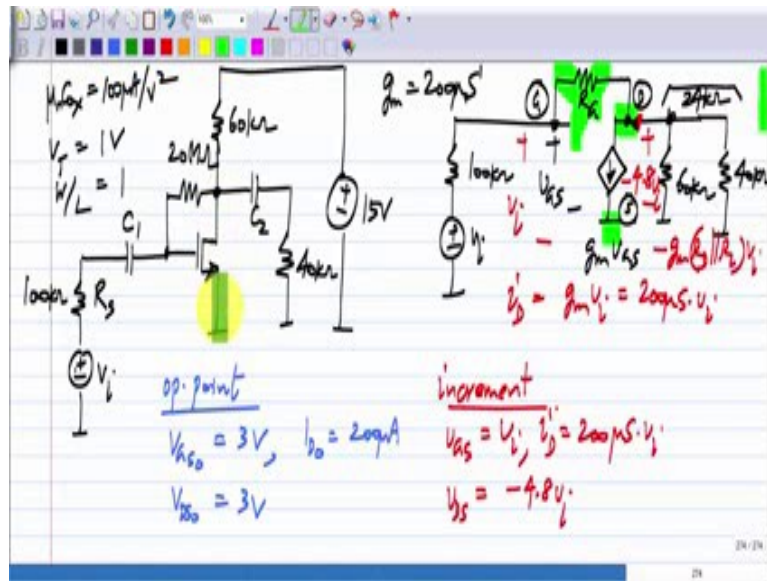
is replaced by a resistor, I had mentioned earlier that many times you do not want to use current sources but you use resistors for biasing especially in case of discrete circuits.

So, let say we do that . what resistor do you substitute with you know what current source this is it is $200\ \mu\text{A}$ and you know what voltage drop there is across it. Because for a drain current $200\ \mu\text{A}$, the gates source voltage of the transistor is three volts; and because no current flows through R_G for dc, the drain source voltage is also three volts. So, this point here is at three volts, and this is at the supply voltage of 15 volts. So, there is 12 volts across $200\ \mu\text{A}$; $200\ \mu\text{A}$ with 12 volts across it is replaced by a resistor which is $(12\text{v}/ 0.2\text{mA})$ are $60\ \text{k}\Omega$. So, I will do that so $60\ \text{k}\Omega$.

Now let us analyse the swing limits of this. Now the procedure to analyse swing limits is always the same. You first compute the total quantities, $V_{GS(\text{total})}$, $V_{DS(\text{total})}$ and $I_{D(\text{total})}$. To calculate the total, you sum the operating point plus the increment and the increment, of course, comes from small signal linear analysis and that is where the approximation comes in, so that is the approximate part, but that is ok. And then you apply the condition for the transistor going into triode region or to prevent it from going into triode region and to prevent it from going into cut off. And for cut off, we always use the criterion based on drain current as opposed to the gate source voltage.

Now, while evaluating the condition for the transistor going into triode region, you can either use the $V_{DS(\text{total})}$ in terms of $V_{GS(\text{total})}$ or sometimes you can just use the drain and gate voltages, this also has been discussed before. But of course, you have to use the total voltages, not just the quotient voltage or the incremental voltage. The one of these is convenient in some cases, the other one convenient in other cases. So, let us carry out that out for this particular circuit.

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By now you should be quite fluent with calculating the operating point, writing down the small signal picture and doing those calculations on the small signal incremental circuits. So, I will go quickly through those parts of it and spend time on actual calculation of the swing limits. And also because we have been using the same transistor parameters; in fact, I did not even mention that as usual $\mu_n c_{ox} = 10 \mu A/V^2$, and the $V_T = 1V$ and $W/L = 1$. So, that is why for a $200 \mu A$ of current, I have the gate source voltage of $3V$; and this is $60 k\Omega$ and the load is $40 k\Omega$ and these are large ac coupling capacitors. So, the operating point is that $V_{GS0} = 3V$ and $I_{D0} = 200 \mu A$ and V_{DS0} that is quotient V_{DS} is also $3V$, because no current flows through this.

Now, coming to the signal picture so let us say $R_s = 100 k\Omega$ again it does not matter, which is v_i , $100 k\Omega$ and I have the transistor gate, drain, and source. I have this $60 k\Omega$ resistor, I use for biasing; and $40 k\Omega$ load resistor, this is v_{GS} , and this is $g_m \cdot v_{GS}$. You also know having done this calculation many times before that g_m at this operating point is $200 \mu S$. There is the resistor R_G , but we have chosen its value to be so very large that it can be neglected. You can refer to the lesson on common source amplifier using drain feedback to see the constraint R_G are chosen it to be so large that it is negligible. So, I am not even going to include it in any of the calculations, it is as good as it being an open circuit.

And this $20 M\Omega$ is some value I put down, you can even imagine a much higher value like $50 k\Omega$ or whatever. Now the parallel combination of these two $60 k\Omega$ and $40 k\Omega$ is $24 k\Omega$. So, from

this, we can see that the incremental gate source voltage is v_i itself, because no current flows into the gate and R_G so large that no current flows into either. So, I assume that all of v_i appears here just it like it would in a common source amplifier so v_i appear there. The incremental drain source voltage is nothing but $-g_m \cdot (R_D \parallel R_L) \cdot v_i$.

So, this is $-g_m \cdot (R_D \parallel R_L) \cdot v_i$ and in this particular case it is $-4.8 \cdot v_i$, this product is 4.8. And the drain current, again assuming no current through R_G , all of it flows here, and that is equal to g_m times v_i . So, the incremental drain current is g_m times v_i or 200 micro Siemens times v_i . Let me put those things down, the incremental $v_{GS} = v_i$; $i_D = 200 \mu S \cdot v_i$ and v_{DS} which is here between these two it is nothing but the output voltage, it is $-4.8 \cdot v_i$; with v_i equal to zero, here you get the operating point conditions and from this picture you get the incremental quantities. So you add the operating point quantity to the corresponding incremental quantity.

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The image shows a whiteboard with handwritten notes. On the left side, under the heading "Total:", the following equations are written:

$$V_{GS, \text{tot}} = 3V + v_i$$

$$V_{DS, \text{tot}} = 3V - 4.8v_i$$

$$i_{D, \text{tot}} = 200\mu A + 200\mu S \cdot v_i$$

On the right side, under the heading "To prevent M1 from going into triode region,", the following equations are written:

$$V_{DS, \text{tot}} > V_{GS, \text{tot}} - V_T$$

$$V_{DS0} + g_m(B \parallel R_L)v_i > V_{GS0} + v_i - V_T$$

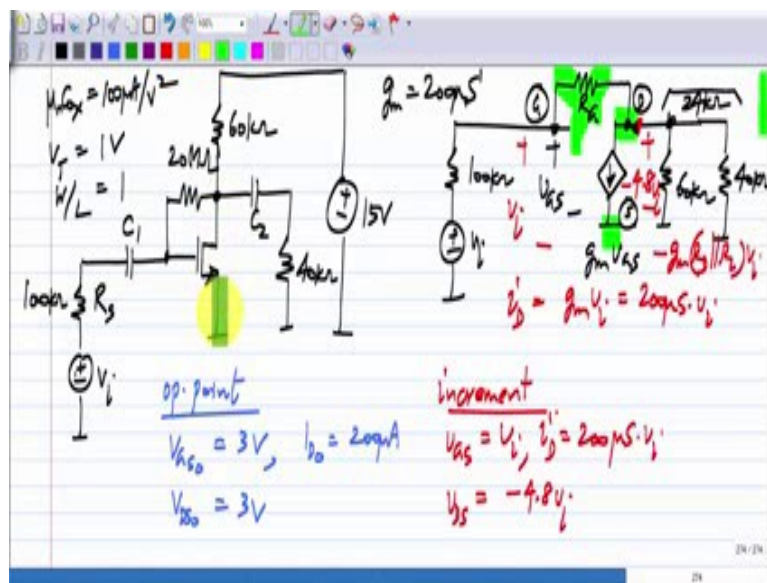
$$v_i < \frac{V_{DS0} - V_{GS0} + V_T}{1 + g_m(B \parallel R_L)}$$

In the bottom right corner of the whiteboard, there is a small video inset showing a man wearing a headset.

So, the total quantities will be $V_{GS(\text{total})}$ is the operating point part plus v_i . $V_{DS(\text{total})}$ is the operating point part $-4.8 \cdot v_i$, that is the incremental part of it and $I_{D(\text{total})}$ is $200 \mu A + 200 \mu S \cdot v_i$. now the cut off due to triode region or to prevent it from going into triode region prevent the transistor M1 from going into triode region i will call this M1 $V_{DS(\text{total})} \geq V_{GS(\text{total})} - V_T$ and the condition is exactly the same as before we are talking about a common source amplifier.

So, what do we have $V_{DS(\text{total})}$ is $V_{DS0} - g_m \cdot (R_D \parallel R_L) \cdot v_i$ and this should be greater than $V_{GS(\text{total})}$ that is $V_{GS0} + v_i - V_T$. So, as usual v_i has to be less than $V_{DS0} - V_{GS0}$, this is the quiescent drain gate voltage how far the drain is above the gate at the operating point plus V_T that is because drain can below the gate by one V_T , but not more than that divided by $(1 + g_m \cdot (R_D \parallel R_L))$, the gate is going up the drain is coming down. So, you have this in the denominator and in this particular circuit V_{DS0} and V_{GS0} are exactly same.

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In fact, that is one of the disadvantages of this configuration using drain feedback because the quiescent drain voltage and gate voltage will be exactly same as each other. So, that means that there is not a lot of room for the gate voltage to rise and drain voltage to fall before it enters triode region. If you had different kind of biasing or somehow modify the biasing, so that this voltage is far above the gate voltage in quiescent condition. Then the swing limit will be higher because the gate voltage can raise by a large amount and drain voltage fall by large amount before the transistor enters triode region.

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Total:

$$V_{gs,tot} = 3V + v_i$$

$$V_{ds,tot} = 3V - 4.8v_i$$

$$i_{d,tot} = 200\mu A + 200\mu S \cdot v_i$$

To prevent M_1 from going into triode region,

$$V_{ds,tot} > V_{gs,tot} - V_T$$

$$V_{ds} + g_m(\beta||R_L)v_i > V_{gs} + v_i - V_T$$

$$v_i < \frac{V_{ds0} - V_{gs0} + V_T}{1 + g_m(\beta||R_L)}$$

$$v_i < \frac{1V}{5.8} = 0.17V$$

So, any way in this case $V_{DS0} = V_{GS0} = 3V$ and $V_T = 1V$. So, it transfer that

$$v_i \leq 1V / (1 + 4.8)$$

$$v_i \leq 1V / (5.8)$$

$$v_i \leq 0.17V$$

. So, v_i has to be below 0.17 volts

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To prevent cut-off of M_1 ($V_{gs,tot} > V_T$)

$$i_{d,tot} > 0 \quad I_D + g_m v_i > 0$$

$$v_i > -\frac{I_{D0}}{g_m} = \frac{-200\mu A}{200\mu S} = -1V$$

Max. sine wave amplitude = 0.17V

cut-off Triode = 0.17V

The graph shows a sine wave with a peak amplitude of 0.17V and a negative peak of -1V. The positive peak is labeled 'Max. sine wave amplitude = 0.17V' and the negative peak is labeled '-1V'.

And if you evaluate the cut off limit to prevent cuts off M 1, $I_{D(\text{total})} \geq 0$. As I mentioned in the previous lessons, another possible limit it is to say $V_{GS(\text{total})} \geq V_T$, but we do not use this limit we use this one. So, which means that

$$I_{D0} + (g_m * v_i) \geq 0 \text{ or}$$

$$v_i \geq - I_{D0} / g_m , \text{ in our case it is}$$

$$- 200 \mu\text{A} / 200 \mu\text{S} = 1 \text{ V.}$$

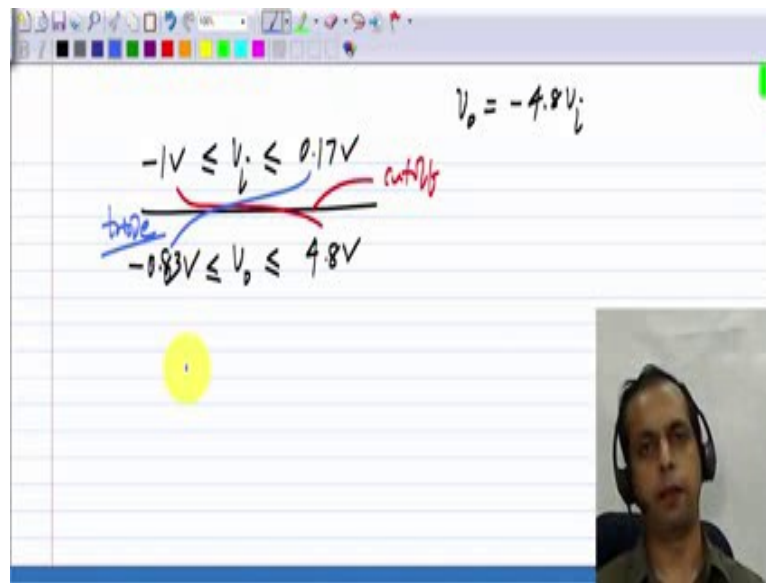
So, the limits for v_i are that $v_i \leq 0.7 \text{ v}$

and this limit is to prevent it from going into triode region and it has to be greater than minus one volt and this limit is to prevent from cutting off.

So, v_i if I plot v_i the limits are some where here the upper limit is 0.17 volts, and the lower limits = -1 V. So, these are the limits and as far as we are concern according to crude approximation within this limit, it behaves like a linear amplifier. We know that as the input amplitude increases, the distortion the non-linear products slowly increase because the small signal or incremental analysis with linear approximation breaks down, but to get an estimate of how much signal we can apply we say that if it is within this swing limits then the amplifier behaves linearly and otherwise it does not. So, you could have any signal which is within this limits and it will behave linearly, but let us say if it goes outside that then in these parts it would not faithful reproduce the input signal.

So, clearly you should avoid this . now if your signal happens to be sinusoidal then obviously, it has to be symmetrical around zero. So, then the smaller of these two limits 0.17 and - 1 will decide the amplitude. So, if you have the sinusoid the only way to fit a sinusoid here is to have an amplitude is either 0.17 volts or below. So, if you are interested in having symmetrical limit which is mostly the case, you should adjust your swing limits so that you do have symmetry. So far all our analyses has focused on the small signal picture, but the swing limits do very much dependent on the operating point. So, we have many options right different kinds of biasing and different values of quiescent V_{DS0} , V_{GS0} etc that could be chosen. So far, we would choose them arbitrarily, but we know their role, they play role in setting the swing limits. So, we have to choose the correct biasing technique, the convenient biasing circuit as well as the correct quiescent parameters to get the optimum swing limit.

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So, let me also write down that maximum sine wave that can be fed in has an amplitude of zero point one seven volts now this cut off limit is one more interesting thing here to see exactly what happens at cut off, we have expressed the limits in terms of the input voltage v_i ,

$$-1 \text{ V} < v_i \leq 0.17 \text{ V}$$

. Sometimes you want know what is the output signal that can be produced so that it is faithful copy of the input and that is very easy to calculate, because we still use the relationship between input and output based on the small signal incremental picture; in our case,

$$V_o = -4.8 * v_i.$$

So, from this, we can write that V_o should be between 4.8 volts which is due to this one, it is

$$-1 \text{ V} * -4.8 = 4.8 \text{ V}$$

so that limit appears here. So, this is due to cut off and on the other side we have

$$0.17 \text{ V} * -4.8 = -0.83 \text{ V}$$

So, if you evaluate the limits in terms of the outputs this is what you will get. So, this is due to cut off and this or this is due to triode.