Analog Circuits
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Module - 06
Lecture – 13

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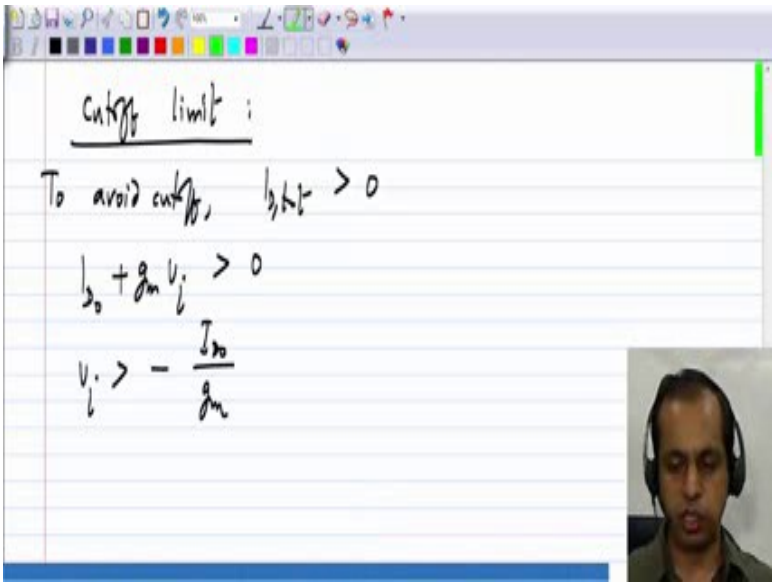

Now, let us look at the limit imposed by cut-off. Now what is cut off , cut-off is when transistor drain current falls to zero. So, to avoid cut off, we must make sure that the total drain current is more than zero. And what is that the total drain current is

$I_{D0} + g_m * v_i > 0$ or

$v_i > - I_{D0} / g_m$.

Now this limit also make sense first of all, this is a negative number, there is some quiescent current in the transistor; and when there is a negative input, the gate voltage falls below the operating point voltage and it tends to move towards cut off. So, it makes sense that this is negative. So, it makes sense that this is negative. So, this will give us some value.

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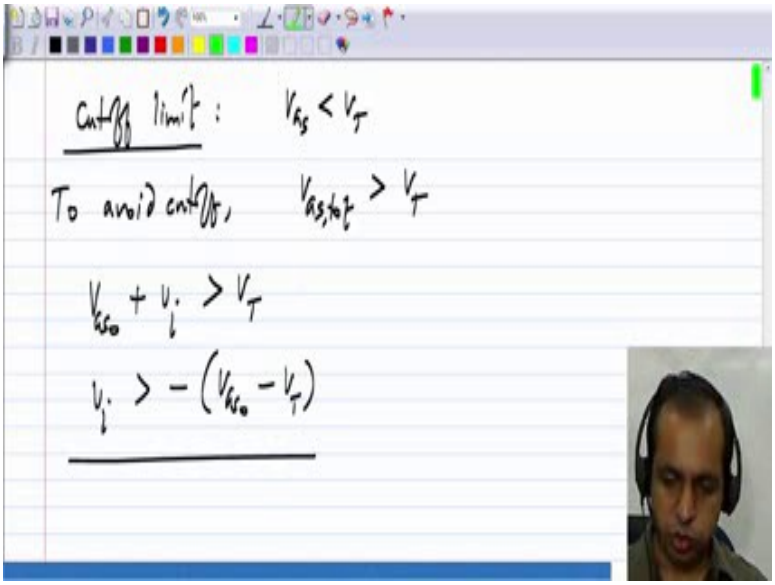

Now, you can also think of cut off as $V_{GS(total)}$ falling below threshold voltage that is to avoid cut off

$V_{GS(total)} \geq V_T$.

And what is V GS total,

$V_{GS(total)} = V_{GS0} + v_i \geq V_T$ or

$v_i \geq - (V_{GS0} - V_T)$

So this is the limit that we get from this is limit that we get by applying cut off condition by saying that $V_{GS(total)}$ has to be more than threshold voltage V_T, so we have two different ways of calculating the cut off limit.

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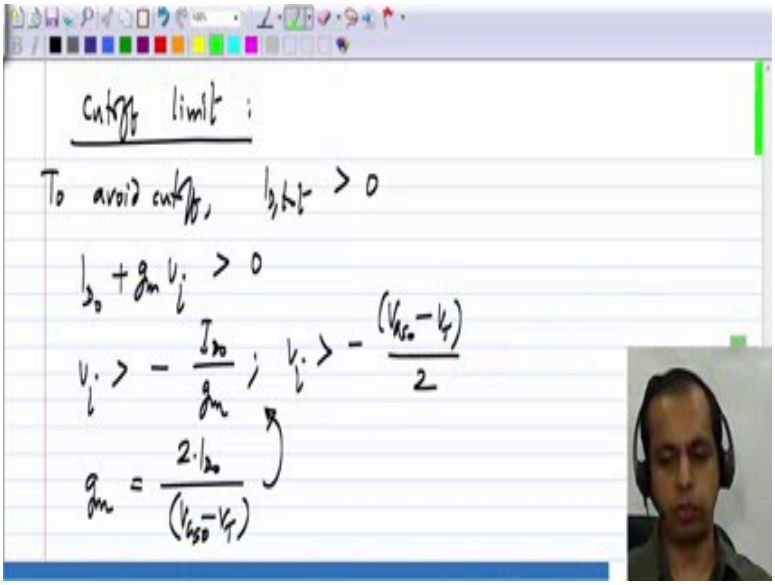

Let us go back to this, now we also know that what is the g_m of transistor; one of the expression for the g_m of transistor ,

$g_m = (2 * I_{D0}) / (V_{GS0} - V_T)$;

So, if I substitute it in there, what will I get , I will get that

$V_i > - (I_{D0} / g_m)$ which is

$V_i > - (V_{GS0} - V_T)/2$

Now this, it has $V_{GS0} - V_T$, just like this one , but there is an extra factor of two. So, first please understand what we are doing, we evaluated the cut off limit in two different ways.

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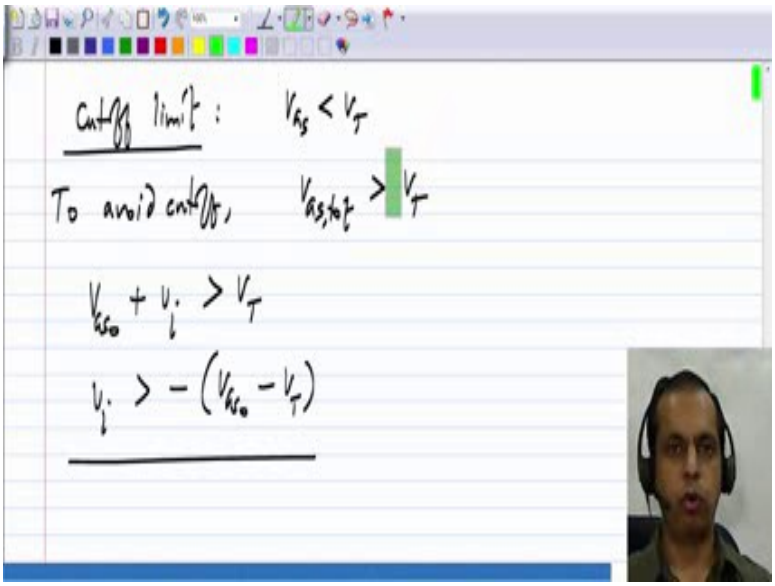

In the case, we have impose the condition that the total drain current has to be more than zero; and in this case, we have impose the condition that the total gate source voltage has be more than the threshold voltage and the two give different answer. Why is that?

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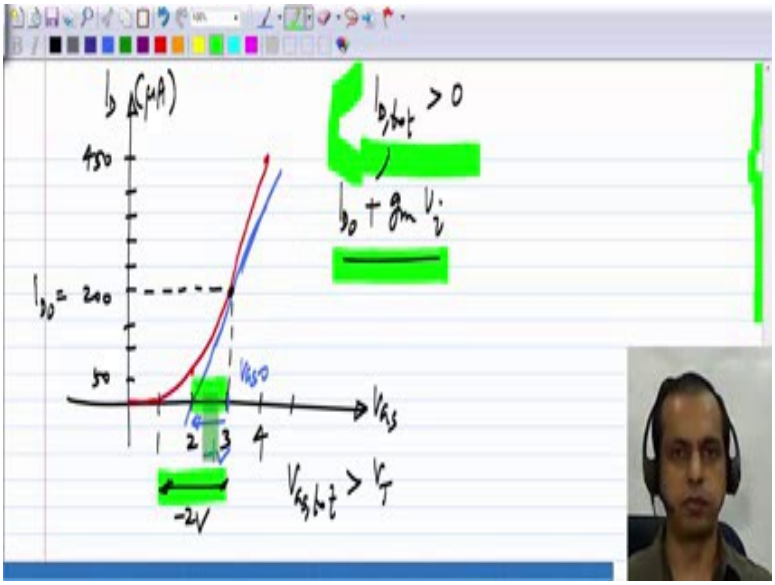

The actual $I_{D(total)}$, $V_{GS(total)}$ characteristics of the MOS transistor in saturation region is square law, this we know. And for all particular transistor, the current is zero up to a gate source voltage of 1 volt, and it increases like that. At three volts gate source voltage, we have 200 μA; at two volts, we have 50 μA, and at 4 volts, we have 450 μA. And our operating point is

over there; the quiescent gate source voltage is three volts; and on top of that, we have an increment. What we are saying is that the total gate source voltage which is three volts plus the increment, it will fall below three volts where v_i is negative. So $3 + v_i$ will be anywhere depending on the value of v_i.

And it when becomes negative, it can reach this point and the current can become zero, so that is a limit that we get by saying that . so we can see that this is an increment of -2 volts and this is the limit we get by saying that the $V_{GS(total)}$ has to be greater than the threshold voltage. Now, we evaluated another limit by saying that

$I_{D(total)} > 0$.

The point is in $I_{D(total)}$, we had the quiescent current I_{D0} which is here in our case plus the incremental drain current was calculated from the small signal equivalent circuit, so plus $g_m * v_{GS}$ or plus $g_m * v_i$.

$$I_{D(total)} = I_{D0} + g_m * v_i$$

In other words, when we say that the total drain current is this, we are really using the tangent to this curve at the operating point. So, we are using the tangent to this curve and when we say that the total drain current is more than zero, we are utilising this tangent and looking at where the tangent goes to zero , not where the original $I_{D(total)}$ vs $V_{GS(total)}$ curves goes to zero. So, the limit that we get by saying that the total drain current should be more than zero is this much and you can see that this is V_{GS0}. So, this corresponds to an increment of minus 1 volt and it is exactly half of this and its nature of the parabola that , so where the tangent crosses zero is exactly halfway to where the parabola actually reaches zero.

So, we have evaluated the cut off limit by using two different criteria; one is by equating the gates source voltage to the threshold voltage; the other by equating drain current to zero, and these two give different answers. Now it so happens that most of the time, we use this as the limit that is we use the total drain current to be more than zero. There are couple of reason for this; although we know that the actual drain current goes zero here we use this. First of all, this gives you a conservative limit and as I described earlier, the swing limit is only a crude estimate of how much signal you can apply. In a real circuit, you have to stimulate the circuit see exactly how much the strength of the harmonics or other distortion products are and then evaluate your signal limit. Here, we just want to crude estimate of the largest signal.

The limit based on the drain current is more conservative that is this gives you a smaller limit compared to the limit based on V GS, so that is one thing. And also it turns out that in case of a MOS transistor, we can use either of this condition. Whereas, in case of bipolar transistor, the condition based on the total current is really what is usable to use the same method for both circuits with the MOS transistors and bipolar transistors; we use the limit based on the total current. This can be confusing but I have told you why the two limits are different. In one case, we are using the parabola; the other case, we are using the tangent line at the operating point; obviously, the tangent line crosses zero at a different point compared to where the parabola reaches zero, but we still use the tangent line although it is approximate, because first of all we only want a crude limit and exactly the same method can be used with bipolar transistors.

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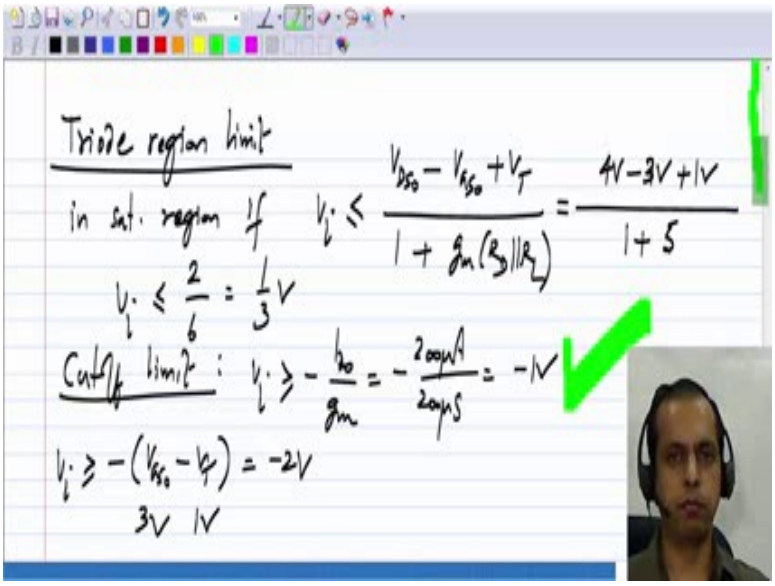

Now, if we do it for our particular circuit what do we get. First the triode region limit; when I say triode region limit, this inequality is written so that the transistor remains in saturation region. It is in saturation region if

$v_i \leq (V_{DS0} - V_{GS0} + V_T) / (1 + (g_m * (R_D \parallel R_L)))$

And how much is this $V_{DS0} = 4$ volts, $V_{GS0} = 3$ volts, $V_T = 1$ volt

$(g_m * (R_D \parallel R_L)) = 5$

$1 + (g_m * (R_D \parallel R_L)) = 6$

$V_{DS0} - V_{GS0} + V_T = 2$

$v_i \leq (2 / 6) = 1/3$

So, if the inputs volt is greater than about 330 milli volts, the transistor will go into triode region.

And the cut off limit, if you use the drain current criteria, we know that

$v_i \geq - (I_{DO} / g_m)$ or

$v_i \geq - 200\ \mu A / 200\ \mu S = - 1$ V.

And if you use the $V_{GS(total)}$ based limit,

$v_i \geq - (V_{GS0} - V_T)$;

$V_{GS0} = 3$ V , $V_T = 1$ V, so this says that it

$v_i \geq - (2$ V)

And like I described earlier this gives a conservative limit and this method can also be used with bipolar transistors. So, we will use this one. So, what this whole exercises saying is that is if , v_i is between -1 V and +1/3 V, the transistor remains in the desired region of operation and everything works properly, but if it goes beyond these limits then the transistor will either enter the triode region or the cut off region.

So, this gives us crude estimate of how largest signal we can apply. We know that our devices are non-linear. If you apply indefinitely large signal to a circuit that contains transistor, you will have very large non-linear products and the circuit will be unusable. So, we want an estimate of how much signal can be applied and this gives us a crude estimate that does not depend on criteria like this distortion which is much harder to evaluate and nearly impossible to do by hand. You use a circuit simulator for that one.

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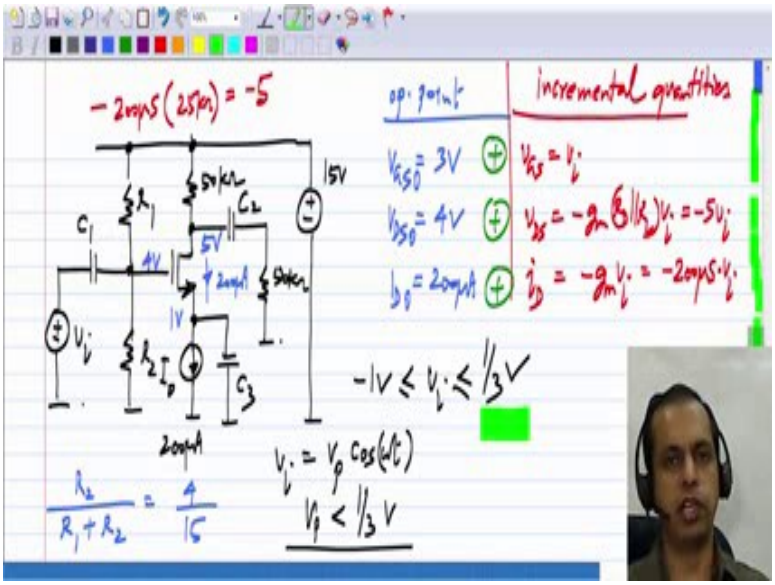

So, to go back to our circuit; so in this circuit,

$-1\ V \le v_i \le 1/3\ V$

Let say v_i is a sinusoid; v_i is V_p *Cos(ωt). Now, this is the symmetrical waveform that is it goes equally in the positive and negative direction. Then what is the largest amplitude that can be applied; obviously, it will be smaller of the two limits, because if you apply an input with an amplitude of one by three volts then at the peak of the sinusoid, this limit will be reached. Of course, if you apply an input with amplitude of one volt, it will cross this limit on the positive side, and the transistor will go into triode region. So, small of these two limits will decide the amplitude of the sinusoid that can be applied. And in this particular circuit, it is the limit due to the transistor entering triode region that limits the signal swing.

So, for this to behave like an amplifier and we will say that for it to behave like a linear amplifier , $V_p \le (1/3)$ V. So, I hope this is clear what we do is calculate the total quantities everywhere that is $V_{DS(total)}$, $V_{GS(total)}$ and the drain current $I_{D(total)}$ and we impose the limits of going into saturation or cut off. But in case of the cut off limit, there are two possibilities to either set the drain current to zero, or the gate source voltage to zero. In our case, we will uniformly use the limit impose by the drain current, we know that it is only approximate; but we are first of all looking only for crude estimate and we also want to use the same method for MOS transistor circuits and bipolar transistor circuits.