Analog Circuits
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Module - 06
Lecture – 11

We have studied a number of basic amplifier topologies so far. In all of these, we drive the input-output relationship using the small signal incremental equivalent circuits which is linear. The input-output relationship is also linear. Now, the MOS transistor is really a non-linear device and we know that the linear approximation breaks down as the signal becomes large. Now, how large is large, it is the difficult thing to determine; as the signal level increases what happen is that the non-linear product go on increasing and at some point they become so large that they are no longer tolerable, so that is how you say how large a signal, you can apply to the amplifier or any other device without running into severe non-linearity.

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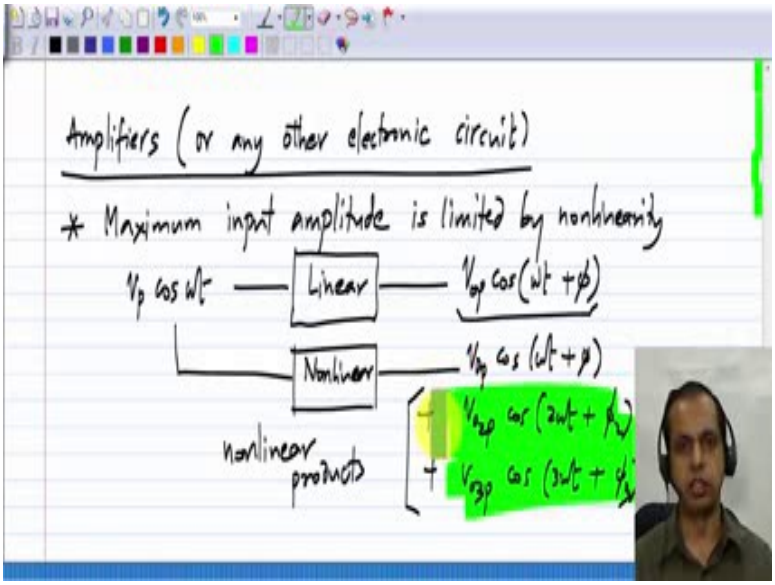

So, in an amplifier or any other electronic circuit, the maximum input amplitude is limited by nonlinearity. As the input amplitude increases, the non-linear products increase. What it means is for instant if you apply $V_{p*}Cos(\omega t)$ to a linear device, the output will be a sinusoid at the same frequency; it may be phase shifted and its amplitude may be different, but they will be nothing else; there only be a sinusoid at the same frequency. But if you do put it into a non-linear device , we know that our amplifier is of course non-linear; we will have a

component at the same frequency as the input, but we will also have in general all the harmonics of the input. This would never happen in a linear circuit, and these are the non-linear products.

Now, as you increase the input signal level, these products will also increase; and at some point, they become quite large and basically you cannot use the amplifier any more. Now, how large the value of this non-linear product can you allow, it is very much depends on the context; it may be one percent of the fundamental, it could be 0.1 percent, so we cannot make the general statement about that. So, in general, what you do is you carry out detail circuit simulation including the non-linearity's; look at the distortion product using usually Fourier analysis. And then you set some limits for the input based on the criteria that you have in one hand; may be in some application, you want non-linear product to have on amplitude that is one by thousands of the fundamental 0.1 percent of the fundamental.

Now, such an analysis requires you to analysis the non-linear circuit as it is; you cannot use the small signal incremental circuit, which is linear. But we would still like to have a way of specifying maximum signal that can be applied to our amplifiers. Let say you take the common source amplifier, you want to be able to say what is the signal level that you can apply. And more importantly, if you are comparing two different designs, let say two people designs common source amplifiers for the same gain, you want to able to compare and say which one can accept a larger signal that is more important. It also important for design, let say you do all of these analysis and determined that you can apply a 100 milli volts input having the non-linear product should be very large. And you want to know how to make it bigger, you want to able to apply like 200 milli volts inputs what do you have to change in the circuit.

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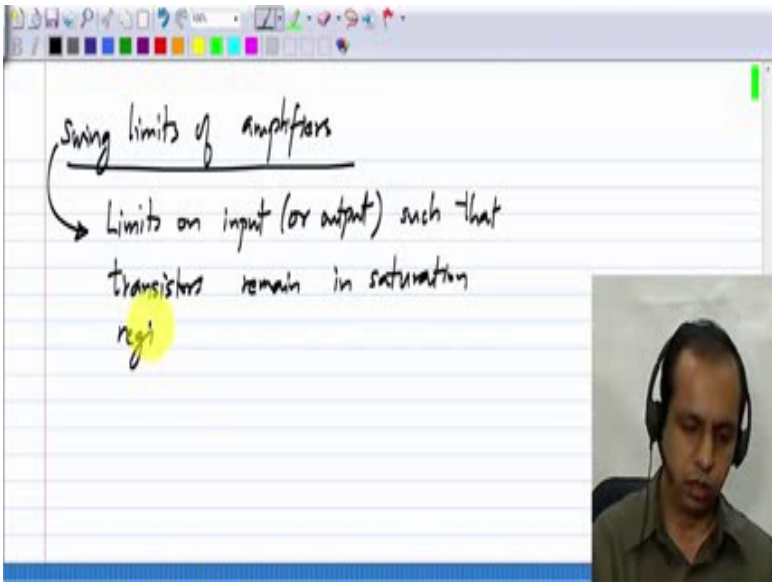

So, this brings us to the discussion of what are known as swing limits of amplifiers. Since, the actual limit is based on the non-linear distortion product and they are very much depends on the context, we will use this swing limits which can be specified without ambiguity for any circuit. And they are based on trying to keep the MOS transistor in saturation region. We know that our MOS transistor has to be in saturation region for it to behave like a good amplifier. So, instead of trying to figure out how much the distortion products is we simply look at the limits on the input signal which will still keep the transistor in saturation region. You can specify the limit in terms of the input signal or the output signal such that all transistors remain in saturation region.

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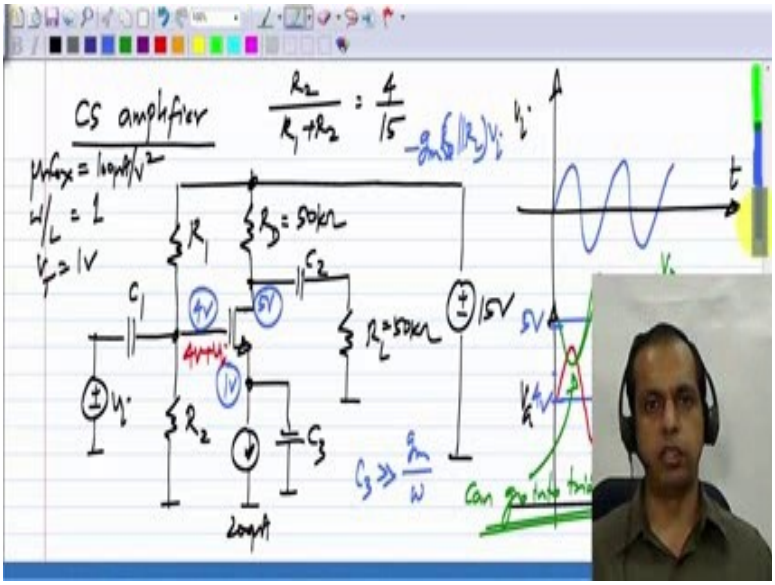

Now, let us takes the common source amplifiers as an example. To avoid the voltage division between R_s the internal resistance of the input source and this R_1 and R_2, I will assume R_s to be zero. This does not change the discussion in any fundamental way. And let me use source feedback biasing and I use large capacitor, so that source terminal is connected to ground, and I have some R_D and some R_L Let me say that this is 50 kΩ and this is also 50 kΩ , and use the 15 volts supply, and this current source is 200 microamperes. Now, I will also assume that all capacitor are chosen correctly so that they behave like short circuit at the signal frequency. So, if you have 15 volts here with 200 microamperes, there is 10 volt drop across R_D, and this voltage with respect to ground will be 5 volts. And I will also assume that R_2 by R_1 plus R_2 is 4 by 15 this means that the bias voltage at the gate of the transistor will be 4 volts.

And you can clearly see that transistor is in saturation region, because the drain voltage is above the gate voltage. If the gate voltage is 4 volts, the drain falls below the gate by one threshold voltage; if the drain falls to 3 volts, it will reach the edge of triode region; and if it is falls further below, it will go into triode region. So, now, it is very much in saturation region. And what is the source voltage, I won't work it out now I am still assuming the same transistor as I always assumed, which is a transistor with mu n C ox of 100 microamperes per volts square and W/L of 1, and the threshold voltage of 1 volt. So, this means that for 200 micro amperes bias current, the gate source voltage of transistor will be 3 volts and the source is at 1 volt.

Now, let see, let us imagine that V_i sinusoidal signal, and we apply the sinusoidal signal to the amplifier. This is the time axis. If I plot the gate voltage V_G operating point voltage is 4 volts. So, let me mark it somewhere over here, it is 4 volts, and over that we have the same signal, the total voltage here will be 4 volts plus V_i because i have R_s is equal zero. So, signal at the gate will be something like that this is V_G when the signal is applied. Now, the drain operating point is 5 volts, so it is somewhere here, this is not necessarily to scale. Now what happen is as V_i increases, V_G will increases; and as V_G increases, the source will be at fixed voltage, because this C_3 is very large it means that the source is incrementally grounded and in the large signal picture what it means is that source will be fixed at one volt.

So, you can think of C_3 has begin a very large capacitor that holds one volt, and it will keep at one volt even when the signal is applied, all criteria that we evaluated that is the C_3 must be much greater than g m by omega and so on. It will ensure that this will remain at one volt, so this does not change at all. So, as the gate voltage increases, the drain current increases; and as the drain current increases, the drain current will flow through R_D parallel R_L, and the drain voltage will fall down. Or you can also think of it as the incremental voltage at the drain is minus gm R_D parallel R_L times V_i. So, the incremental voltage at the drain will be superposed on the operating point voltage which is 5 volts and it does that, it will be out of face of the input and that is how it will be. This is the total drain voltage.

Now you can see that although started off with V_D of 5 volts and V_G of 4 volts, at some point in the cycle, the drain voltage falls below the gate voltage. And for sufficiently large input signal, the drain voltage could fall one volt or one threshold voltage below the gate, and the transistor can go into triode region so that is when it goes out of saturation region, and we take that as the limit. The value of V_i at which the transistor goes into triode region that is one of the limits, so as V_i swings up it can go up into triode region. And similarly, in the other direction, as V_i falls down, you can see that the gate voltage is falling down; the source voltage is fixed. Now, you know that the gate source voltage has to be above the threshold voltage for the transistor to be on. So, it is possible that as the input swings negative, the gate voltage fall below four volts and the V_{GS} of the transistor can go below a threshold voltage, so then the transistor can cut off.

Another way to think about it as, as the gate voltage reduces, the drain current will also reduce; and drain current can go to zero, once it goes to zero that can be future change in the output voltage because the transistor is cut off. As the V_G swings negative, here at these

points the transistor can cut off meaning it reaches the off state. When there is no current at all in the transistor. So, that sets the lower limit for V_i that is the negative limit for V_i. So, there are two reasons why the signal that can be applied to an amplifier can be limited; one is because the transistor can be driven out of saturation region into triode region; the other one is, it could be driven into cut off. Based on these two effects, we will evaluate limits on the input signal. These are the swing limits of an amplifier.