Analog Circuits
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Module - 06
Lecture – 04

We have derived the current controlled voltage source using a MOS transistor, and also analysed it thoroughly in the small signal domain. Now, we need to find a suitable bias circuit for it and complete the picture.

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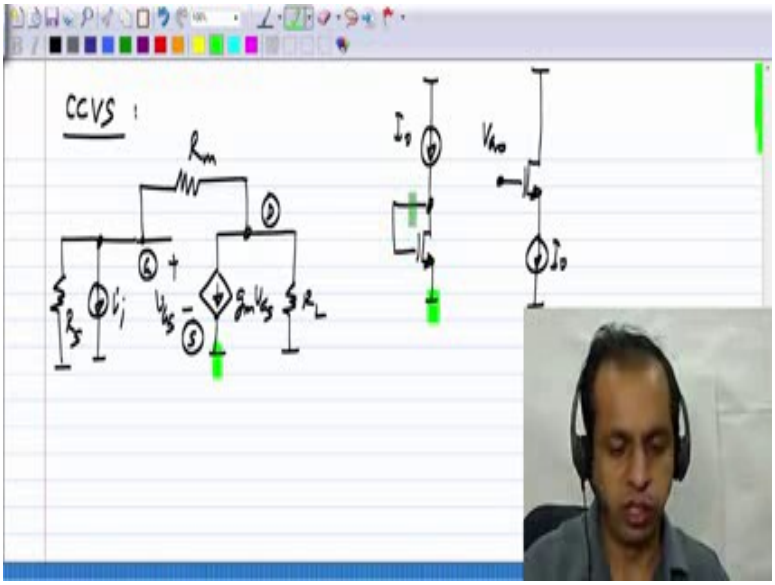

The small signal picture of the current controlled voltage source is this, i_i and R_s, and this is connected between the gate and source of the MOS transistor. We have v_{gs}, we have the load R_L, and the resistance which realize the trans resistance is R_m connected between drain and gate. Now, the source is grounded here. So, it is more convenient to pick a biasing technique where the source is already grounded. Now, if we leave aside two of the biasing schemes, which require an op amp, we have either drain feedback, which looks like this or source feedback which looks like that.

Clearly, the drain feedback configuration appears very suitable for this. First of all, the source terminal is connected to ground. Now we have a resistance R_m between drain and gate, when we came up with the biasing technique, we had no specific requirement. So, we just connected the drain directly to the source, but it does not have to be like this. We can always

insert a resistor in this branch and nothing will happen, because the gate current is zero and the biasing will not be disturbed at all. So, this is suitable for this and actually the resulting topology looks very similar to a common source amplifier with drain feedback bias. So, we will use this biasing techniques the only thing we have to change is that between drain and gate, we cannot make a direct connection we have to connect a resistor R_m that is all that there is to it.

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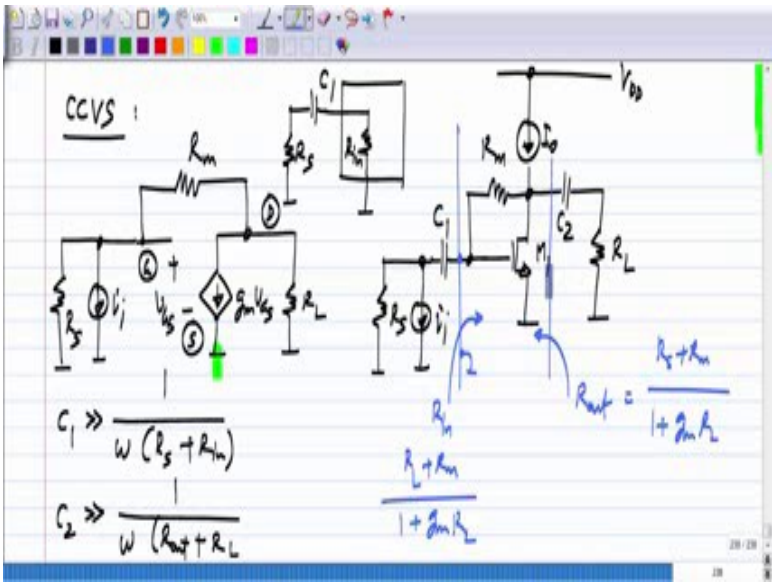

So, we have the supply voltage and a current source I_O, and we connect this resistance R_m like that. And as usual, the input source is ac coupled through a capacitor C_1, and the load is a ac coupled through a capacitor C_2. So, this is the complete picture of a current controlled voltage source, and it looks exactly like a common source amplifier with drain feedback bias except here we show a current source in parallel with the resistance, because it is a current controlled voltage source. As long as this resistance is there, you can also equivalently show it as a voltage source in series with a resistance. So, it is exactly the same circuit; the only difference between this and the common source amplifier with drain feedback bias is in the value of R_m and the constraints.

In case of common source amplifier using drain feedback, the value R_m is made very large whereas now it not so large. So, this circuit is very simple and I do not think I need to discuss this any further, you can evaluate the operating point of this; you can write the small signal picture assuming C_1 and C_2 are shorts and find the gain. We have actually already done that.

Now the only thing remaining is to figure out values of C_1 and C_2 such that they do behave like short circuits. And for that it is very easy I am not going to go through all the steps, but you have to realise that the resistance looking that way between this point and ground is nothing but the input resistance that we have already evaluated. We know that this is $\frac{R_L+R_m}{1+g_{mR_L}}$, and of course, in this it is implied that C_2 is chosen correctly, so it behaves like a short circuit. And similarly the resistance that looks back this way is R_{out}, and we know that it is $\frac{R_s+R_m}{1+g_m R_L}$.

So, what is the condition for C_1, you can see that if you deactivate the circuit across C_1 you will see R_s plus R_{in}. Inside the circuit, we have R_{in}; and C_1 is connected here; R_s connected there to the ground, and this is ground. So, across C_1, you have R_s plus R_{in}. So, the reactance of the capacitor C_1 must be much smaller than the resistance that is across it or $C_1 \gg \frac{1}{\omega\left(R_s+R_i\right)}$. And similarly, across C_2, you see R_L; and you see the output resistance of the circuit which is R_{out}. So, $C_2 \gg \frac{1}{\omega\left(R_{out}+R_L\right)}$. So, you see R_L on this side and you see R_{out} on this side. So, C_2 must be much more than that one.

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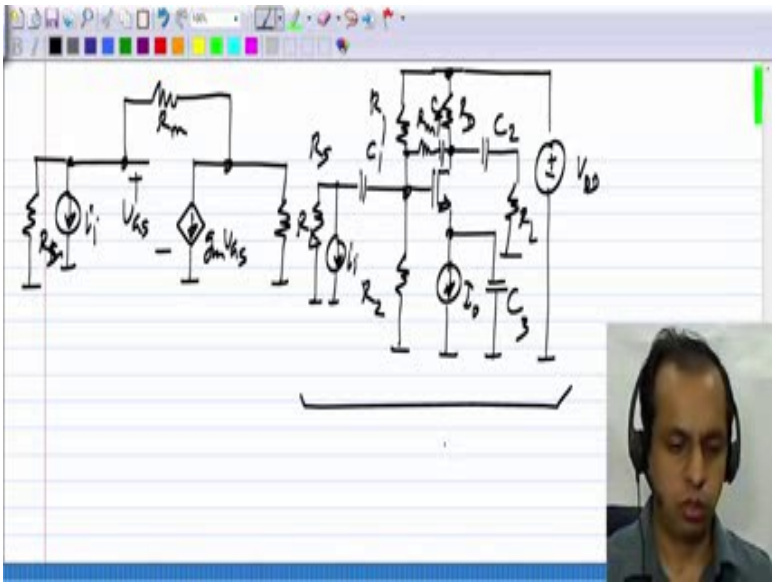

Now, we can also realise this current controlled voltage source using source feedback bias. Again the signal picture of the current controlled current source is this. If you use source feedback technique for biasing, we will have I_O, we have the supply voltage and we have some fixed voltage V_{GO}. This is not the most convenient bias circuit for the current controlled voltage source, but just to see how it is done we can do that. First of all, drain here is not connected to small signal ground, whereas here the drain is connected to V_{DD} which means it is the small signal ground, so that is one problem.

And then, but we have dealt with that kind of situation before and then here the source is not at ground, whereas here the source is at ground so that has to be fixed as well. So, let us do all of that. First of all, this V_{GO} has to be derived from the supply. So, we use our usual resistive divider to do that, and then the input has to be connected to the gate without disturbing the bias. So, as usual, we use ac coupling, we cannot connect the drain directly to the supply voltage, because that will be short the drain to ground in the small signal picture. So, we have to connect through a bias resistor R_D as usual, and also the load resistance has to be ac coupled to the drain node, so let me call this C_2.

And finally, we have to have a resistance between gate and drain in the incremental picture, again of course, everywhere we have assumed that the input signal is at some frequency greater than zero that is it is not a dc input. So, you have to connect between drain and gate but we should not connect directly because that would disturb the bias that will actually

introduce drain feedback. So, we ac coupled that as well, we connect a capacitance in series, but the idea that this capacitance behaves like a short at signal frequencies. So, for signal frequency, it is as though only R_m is connected between drain and gate, so this is R_m. And finally, the source terminal has to be grounded, and we know how to do that we have used it for common source amplifiers, we can connect a capacitor to ground. So, we have four capacitors, but that is ok. So, this is just show that you can use this source feedback bias also for the current controlled voltage source.

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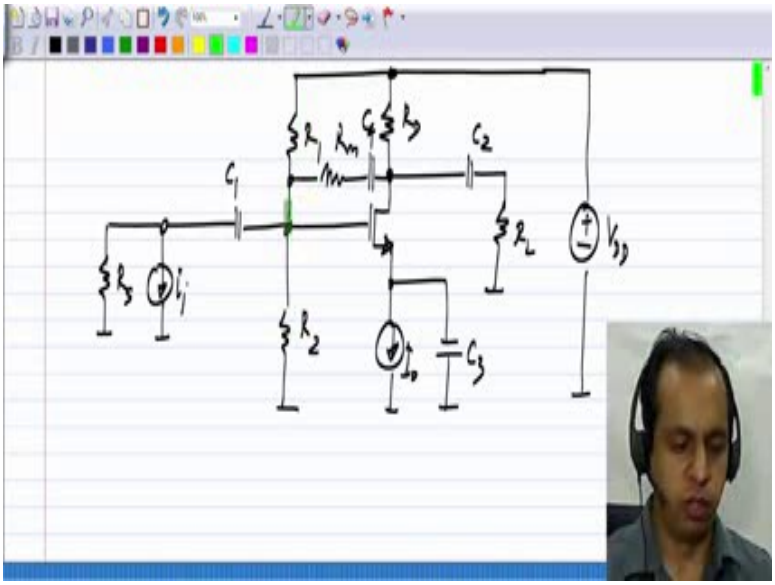

So, let me draw this little more neatly. This is the input source; it is ac coupled to the gate of the transistor; from the source we have a current source I_O which is by passed to ground using another capacitor. We have the drain bias resistor R_D, and resistance R_L, this is the supply voltage V_{DD}. Finally, we have the resistor that realises is the trans resistance R_m in series with a capacitor so C_1, C_2, C_3 and C_4. C_1 and C_2 we have already evaluated; C_3 similar to what we needed for the common source amplifier; C_4, I would not do it now; you can take it as an exercise and do it yourself.

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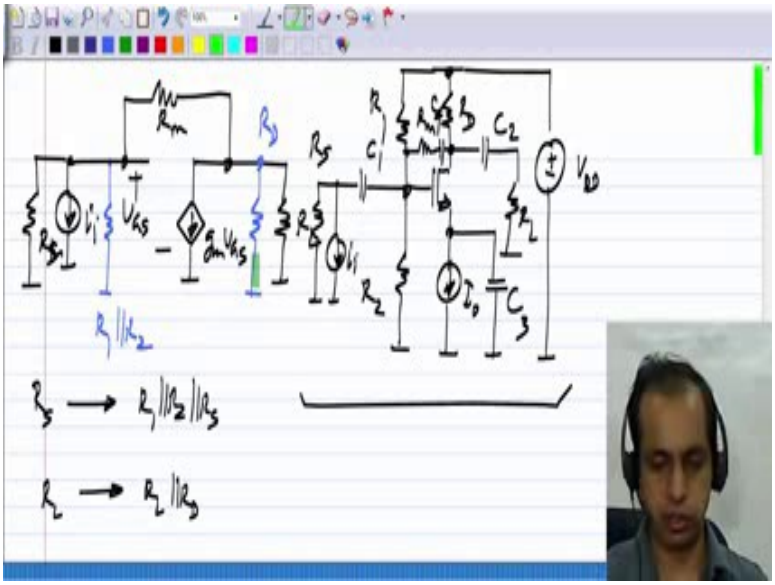

There are two extra components here we have R_1 and R_2 from gate to ground, that is we have $R_1 \parallel R_2$ between the gate and ground. First of all, by choosing R_1 and R_2 to be very large much large than R_s, you can completely neglect the effect of it, because if R_1 and R_2 are much large than R_s, the effective resistance between gate and ground will still be R_s. And it that is not possible then wherever you had R_s before in your expression, you have change it to $R_1 \parallel R_2 \parallel R_s$. Also we have drain bias source R_D, so that introduces an additional resistance from drain to ground. So, wherever we had R_L before, it has to be replaced by $R_L \parallel R_D$ in our analysis.

And in practice, it is not difficult to make R_1 and R_2 very large, so that they can be neglected whereas it is not quite possible to R_D is very large because in that case the voltage drop across this becomes very large, and you have to use a very large supply voltage. So, this will affect circuit to some extent, but because it is a current controlled voltage source, the output voltage should not depend so much on the load resistance. So, it will be affected, but not by much. As long as the trans conductance g_m is very large.

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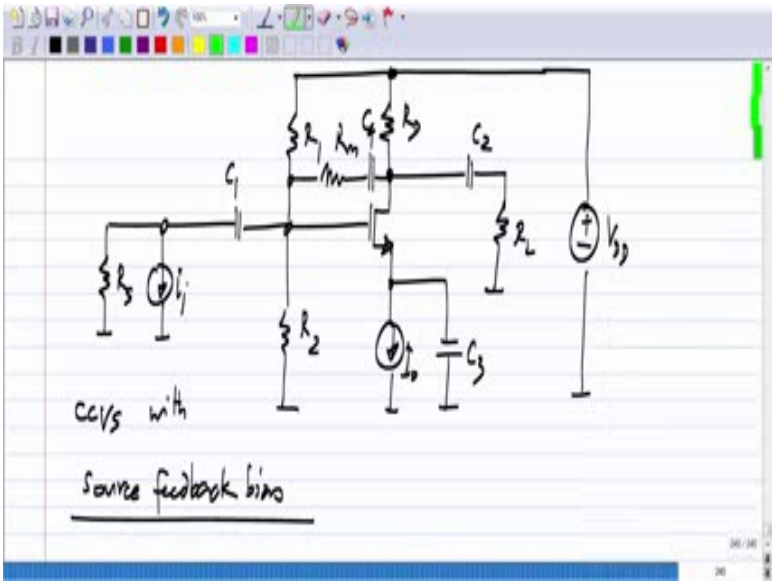

So, this is a current controlled voltage source with source feedback biasing. So that completes the picture of the current controlled voltage source. And we have also illustrated that we can combine at with the two biasing techniques drain feedback and source feedback.