Analog Circuits
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Module - 05
Lecture – 14

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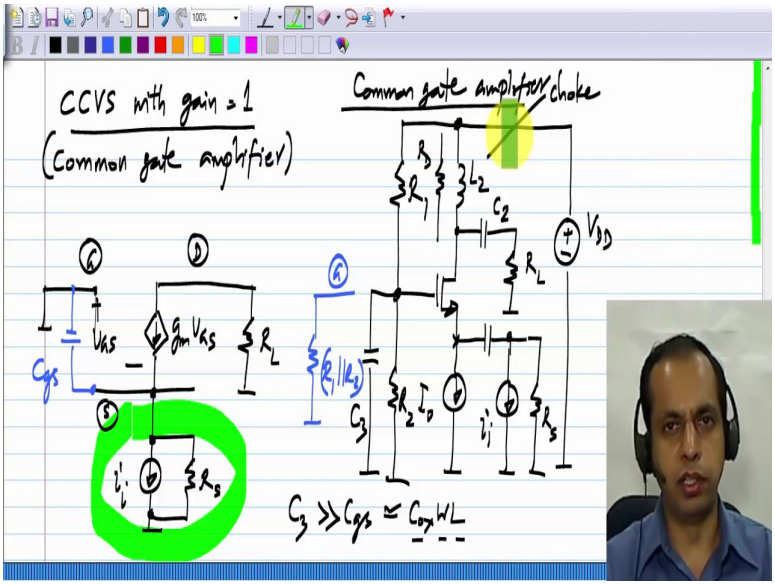

We have derived the small signal picture of a current buffer or a common gate amplifier, it is a current controlled current source of gain one. Now, we will combine it to the suitable biasing arrangement to complete the circuit. The gate of the MOS transistor is grounded, the input is connected to the source terminal. And the output is taken from the drain and I'll for now assume that there is a load resistance connected that way. This is of course, $g_m v_{gs}$. Now, what biasing arrangement suit this, like before because the source terminal is not connected to ground, we use source feedback biasing. In source feedback biasing, we connect a current source to the source terminal and the drain just for biasing purposes is connected to the supply voltage V_{DD}, and the gate is biased with a voltage divider R_1 R_2, which is powered from V_{DD}.

Now, to this biasing picture, we have to combine this signal picture. So, first of all, the input is connected to the source. And we will assume as usual that the signal frequency is above a certain value, it does not include dc, so we can couple it through a capacitor. We will assume that it is connected like this. And then the load has to be connected between drain and ground,

here the drain is connected to V_{DD}, which means it is connected to small signal ground or incremental ground in the incremental picture. It has to be removed from that and connected to the load, and again if the signal is above a certain frequency, what we can do is, we can have an inductance L two, whose reactance is much more than the load resistance and we can ac couple the load resistance. This is the exact same arrangement we used with the voltage controlled current source.

Now, of course, if inductors are too bulky and we cannot use them, we can replace L_2 with some resistor R_D, and if you do that of course, only a fraction of the current can flow through R_L, because you cannot make R_D indefinitely large, that will mean making the supply voltage V_{DD}, very very large as well, so that is not reasonable. So, you will end up having to share the current between this drain bias resistor R_D and the load R_L, but you know how to analyze that, so, I am not going to go through that in detail. You can either use this L_2, which is the large inductance. By the way, whether the inductance itself is large or not depends on the frequency as well. The reactance of this has to be much more than R_L. If you go to very high frequency, a small inductance has a high reactance. So, it is quite common to see a picture like this, in high frequency circuits. In low, frequency circuits, the required value of inductance becomes so large that you do not use it. .

And many times this inductance which is very large, it is referred to as a choke. Essentially, there is no current flowing through this, you can think of it as choking the current that is going into the small signal ground, and letting it all go into the load resistor. And the gate has to be connected to small signal ground, and if you look at it, it is connected to ground through R_1 and R_2. The actual picture looks like this; the gate terminal is connected to ground through this. Now, so far, we have been assuming that the gate current is zero, so if the gate is zero, even if you have a resistance between gate and ground, this will be at zero volts. So, that is seems adequate, but it turns out that and we have not studied this part yet, there is a capacitance between gate and source. There is a capacitance refered to a c_{gs} between gate and source.

So, because of that if you connect it up just like this, that is it is connected to ground through R_1 and R_2, the gate voltage will not be exactly zero for signal frequency. It will be at zero voltage for dc increments, but for signal frequency it may not be exactly at zero. So, we always connect a capacitor also, a large capacitor, let me call it C_3 between the gate and ground that make sure that the gate is connected to ground. Now, we have not studied the

transistor model including this capacitance, but take it from me that in a common gate amplifier, you do connect a capacitor from gate to ground. And how much should this be, it should be much more than c_{gs} of the transistor, and c_{gs} of the transistor is order of $C_{ox}WL$. You are familiar with these terms C_{ox}, W and L, from the MOS model.

Now, of course, because we have not studied these things. As far as we are concerned, we will assume that we will always connect the C_3 that is very large, so this point is shorted to ground for signal frequencies. So, this is now the complete common gate amplifier with biasing. You can see that the output part of it, resembles what we had for the voltage controlled current source, that is not surprising, voltage controlled current source and a current controlled current source, the output parts are the same, so it looks nearly the same.

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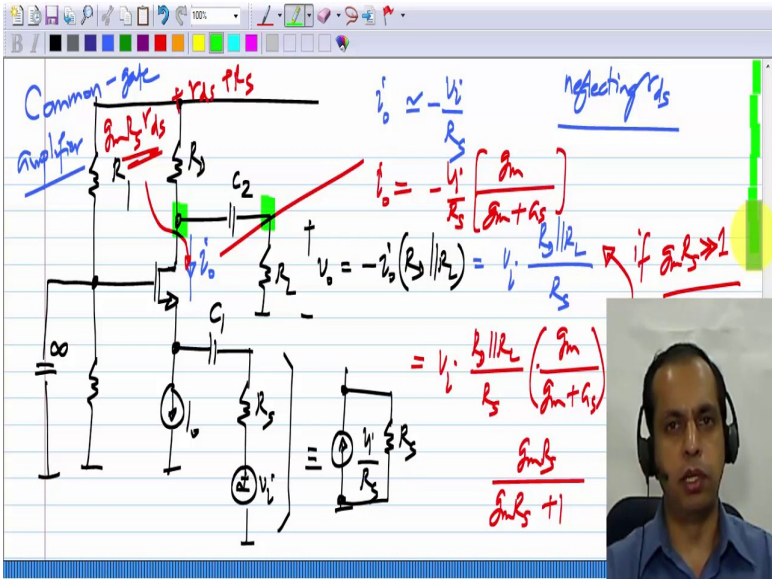

Now, let me put the circuit down again. I will show this as infinity meaning it is so large that, it is short circuit. And I will show a resistor R_D instead now, and we can also have another R_L here. Now, we connected a current source at this point, but many times people like to operate with voltages; so even though it is a current controlled current source, we connect a voltage source in series with a resistance. So, v_i in series with R_s, now of course, you know that this part of it is equivalent to having a current source $\frac{vi}{Rs}$ in that direction. Keep in mind the direction for current we have been taking here, is going downwards whereas, if I have v_i with

upper terminal positive it will be upwards in parallel with a resistance R_s. So, it behaves in exactly the same as before.

And this current here, is approximately equals to $\frac{v_i}{R_s}$ or rather – $\frac{v_i}{R_s}$ because the polarity of this is reversed. In this case, this current here i_o was approximately equal to the input current, but the input current is pointing downwards, so in this case, $i_o \sim -\frac{v_i}{R_s}$. And if you again take the output voltage instead of the output current, what will this v_o be, it will be $-i_o(R_D||R_L)$. This is assuming C_2 is large enough to be short circuit and so on. If that the case, then the output voltage with a voltage source input will be $\frac{v_i(R_D \vee ¿ R_L)}{R_s}$. So, you can use it with a voltage input, of course, in this case, you can see that the gain depends both on the load resistance and the source resistance. Just because you apply a voltage input and take voltage output it does not mean this is the voltage controlled voltage source.

A good voltage controlled voltage source should also have a very low output resistance and a very high input resistance, this has exactly the opposite. The input resistance is very low, and the output resistance is very high, so this is really a current controlled current source, but you can operate it with a voltage source in series with the resistance and also consider voltage as the output. In that case, the gain will be some resistor ratio, which can also be accurately set and it is sometimes use like this. So, when you see this common gate amplifier you do see sometimes with voltage input and the gain is this one. Of course, this is the approximate gain. If you use the exact value, again I have neglected the r_{ds} of the transistor, as I said r_{ds} is important for the output resistance for the other things it make the small change and nothing else.

Now, we know that this $i_o \sim -\frac{v_i}{R_s}$, but it is really $-\frac{v_i}{R_s}\left(\frac{g_m}{g_m+G_s}\right)$. So, this number is close to one, but not exactly one. So, the actual output voltage will be $\frac{v_i(R_D \vee ¿ R_L)}{R_s}\left(\frac{g_m}{g_m+G_s}\right)$.

And this also can be written as $\frac{g_m R_s}{g_m R_s + 1}$. So, as long as the $g_m R_s >> 1$, it reduces to this, if $g_m R_s >> 1$, so that is it about the common gate amplifier. It is a current controlled current source with gain one, and it is current buffer. So, what it does is it takes a rather poor current source, this current source has a resistance R s and it gives you the same current, but with much higher resistance.

Looking in here, you know that the resistance is $g_m R_s r_{ds} + r_{ds} + R_s$, because of this term, the resistance looking in here is much higher than R_s. So, it gives you much better current source. And it is exactly like the voltage buffer, the voltage buffer can take a voltage source with a high series resistance. And make it look like a better voltage source, the same voltage, but with the much smaller output resistance. So, this current buffer serves the similar purpose. And it is also a very widely used building block.

Now, as far as capacitance values are concerned, we already calculated these things, so I am not going to go through that, the value of C_2, we have calculated it so many times. If you want C_2 to be like short circuit, so that the output voltage is the same as replacing C_2 by a short circuit then the reactance of the $C_2 << R_D + R_L$. But if you want the drain voltage and the output voltage to be nearly the same then the reactance of the C_2 must be much smaller than R_L by itself. And similarly, you can calculate it for C_1, reactance of C_1 must be much smaller than what appears across it, which is $R_s + \frac{1}{g_m}$. I assuming we can calculate these things because we have calculated these things in other context, so I am not going to go through that again. So, that completes the current controlled current source or the common gate amplifier. Again common gate amplifier is usually presented as basic building block, now we would like to think of it as a feedback network which forces the output current to be equal to the input current by adjusting v_{gs} appropriately.