Analog Circuits
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Module - 05
Lecture – 12

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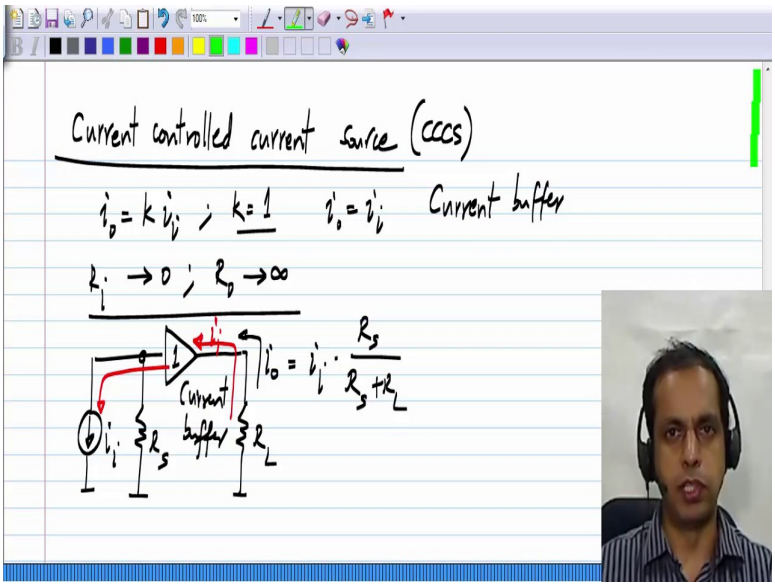

Now, we will take up another type of controlled source, which is the current controlled current source. And just like with the voltage controlled voltage source, we will make the gain of the current controlled current source to be one, that is in general a current controlled current source should have an output current which is some constant k times the input current, and this should be independent of the impedance of the source which is driving the current controlled current source and also the load resistance. For that to happen, it should offer a very small input resistance tending to zero, and a very high output resistance. Now, because of the way the MOS transistor is, which has a common terminal between control and controlling side that is the source terminal is common to the two sides, it turns out that we can only realize k equals one.

So, we will try to realize $i_o=i_i$. Again as with the case of the voltage controlled voltage source, although there is no gain, this is still useful as a current buffer, meaning let say we had an imperfect current source i_i in parallel with some source resistance R_S. And if you have a load resistance R_L, if you connect it directly, the load current will be just a fraction of the input current. And how much this fraction is depends on the ratio R_S to R_L. Now, if you use a

current buffer, this is a current buffer, it will have a very low input resistance meaning all of that current will go into the input and the output current will be exactly equal to the input. So, regardless of the values of R_S and R_L, the output current – the current in the load will be equal to the input current, so that is the use of it. And we will realize this using a MOS transistor.

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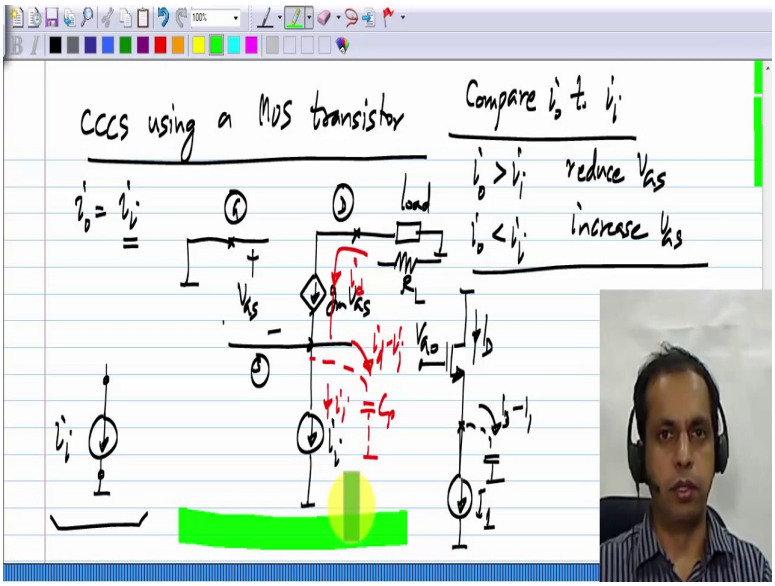

So, we want $i_o=i_i$, when we say there is an input current; obviously, we mean that there is a current source whose value is i_i; and of course, it could be non-ideal. In fact, it is expected to be non-ideal. And it will have a resistance in parallel with it which is R_S. Recall that our representation for a voltage input is a voltage source v_i in series with resistance R_S, equivalently you can think if it is a current source i_i in parallel with R_S. So, this is our input. Now, in the initial discussion, just to make that drawing I will omit R_S. Although later I will put it in and analyze its effect.

Now, I want $i_o=i_i$. And what is this i_o, we have the MOS transistor with its gate, drain and source terminals. This is v_{gs}, and this current is $g_m v_{gs}$. And the incremental drain current flows from drain to source, and that will be the output current i_o, so that is where a current flows in a MOS transistor, and that has to be the output current of our circuit. So, this current flows from drain to source. Now, what we do in order to realize a current controlled current source, we have to compare the i_o the output current to i_i. And if $i_o > i_i$, we have to reduce v_{gs}; and if $i_o < i_i$, we have to increase v_{gs}. Now, eventually the output current of this block must be

connected to a load, so the current flows from drain to source, we could connect the load to one of this terminals, and do this comparison at the other terminal.

Now, if you have been kind of following closely and you recall what we have done in earlier lecture, you see that we have actually done this already. What we are saying is that the drain current of the MOS transistor i_d here let me rename this i_d, we want to make it equal to i_d or $i_o=i_i$. Now, where have we done this before, we have made the drain bias current of a MOS transistor equal to the given current i_o, that we have already done. So, we have done it for the sake of biasing, now we will do it for signals. Now, it turns out that the most convenient way of doing it for signals is to essentially copy the source feedback biasing.

What do we do here, we had a certain drain current I_D, and we want to make it equal to a given current source let me call it just to not confuse with other i_o, let me call this I_1, we want it to make $I_D=I_1$, we connected these two together, so that the difference flows into a parasitic capacitor. And if I_D is more than I_1, it increases the source voltage, thereby reducing the value of I_D. The gate is connected to a fixed voltage. And if I_D is less than I_1, current will be drawn out of the capacitor, the source voltage will fall down, V_{GS} will increase and the current will increase. Now, this is a convenient way of doing it with signals as well.

So, what we have to do, the drain current of the MOS transistor is flowing like that. And we connect our desired current, in this case, it is the input current, so we call it i_i there. So, what happens, we have i_i over here, and i_d over there; the gate is connected to small signal ground. Here it is connected to some fixed voltage, but in this case, we just connect it to ground. Now, what happens, you can imagine exactly the same thing happening as earlier, you can imagine a parasitic capacitance here, and this difference i_d - i_i will flow into that one. And what happens if initially i_d was too small, then this current will be negative, so current will be pulled out of C_p, the source voltage will fall down, v_{gs} will increase and i_d will increase. And exactly the opposite happen i_d is too large.

Now, i_d is flowing from drain to source, so we can use the part that is flowing out of the drain to connect it to a load, that is a load and for illustration you can imagine that it is a resistance, so that is all that is there to it. In this case, I did not discuss this scheme in too much detail, but making the output current or drain current of a transistor to a given current i_i, we already done it before for the sake of biasing. Here we have made this total current I_D equal to this given current I_1.

Now, what applies for total current definitely applies for incremental currents and we used exactly the same scheme. The negative feedback action must be pretty obvious by looking at how much current flows into this C_p and it depends on the difference i_d - i_i. So, this is our current buffer or current controlled current source; or at least this is our attempt at getting one such block. Now, you can see that in steady state, no currents flow through the capacitor and all of these i_i will flow through here. What it really means is that v_{gs} will adjust itself so that the current flowing here g_m times v_{gs} equals i_i. Now, we can analyze it further to see whether it really does that and also to see what its input and output resistances are.