Analog Circuits
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Module - 05
Lecture – 10

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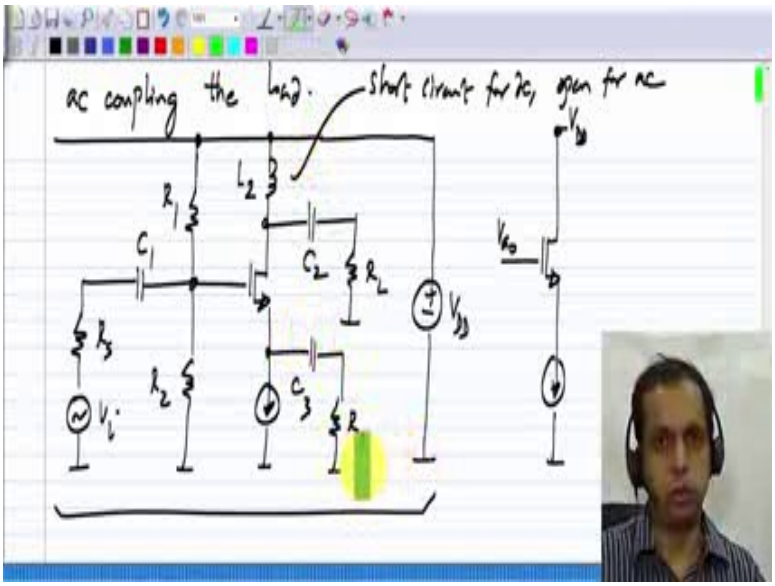

Let me redraw the picture I had, and let me show a load which can be connected only to ground. Now in the biasing picture, gate is connected to V_{G0}, and drain is connected to V_{DD}; in general, it has to be connected to some point such that it remains in saturation region. So, let us say we want to connect it V_{DD} that is for dc that is for dc biasing, but we want it take to get disconnected from V_{DD}. If it is connected to V_{DD} even for signal frequencies the drain current, simply goes into ground, small signal ground. So, it has to become an open circuit for ac or higher frequencies. So, whatever you connect here should be a short circuit for dc, and open circuit for ac.

And what is such an element, the obvious choice is the inductor; I will call it L_2. And this drain must get connected to the load only for ac, it should not get connected for dc. So, we need for open circuit for dc. So, we use the familiar coupling capacitor C_2. Now how do we evaluate the values of L_2 and C_2, you can write down the transfer function and evaluate it, but I will take an easier way and do it kind of step by step. Let me draw the small signal picture of this, and while drawing that, I will assume that this C_1 and C_3 are already shorted and so on. Our interest is now is to only to find values of L_2 and C_2.

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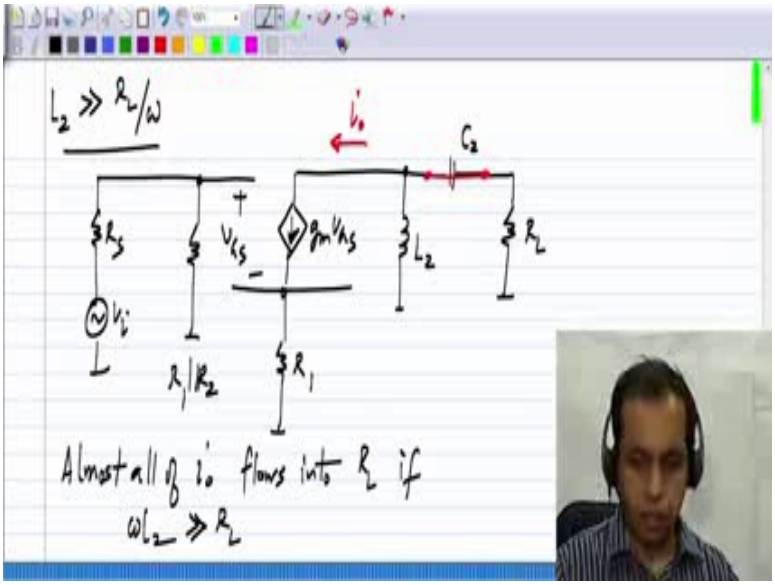

Between the drain and small signal ground, we have L_2; and between that and the load, we have C_2, then we have the load resistance. Now, first I will assume that C_2 has been chosen correctly so that it is a short circuit. If I do assume that C_2 is a short circuit then how to evaluate L_2, basically my output current is this i_o that is flowing through the drain of the transistor and I want all of it to go into the load. So, all of this I naught must go through the load, it should not go into L_2. And L_2 and R_L are in parallel if C_2 assumed to be a short.

So, how do you make all of i_o or most of i_o go into R_L. The reactance of L_2 at the signal frequency must be higher than resistance R_L. Almost all of i_o flows into R_L, if ωL_2 where omega is the signal frequency and ωL_2 of course is the reactance is much more than R_L. So, we have a parallel combination of impedances and one impedance is much higher than the other. So, all of i_o will go into R_L, so that is how you have to choose L_2. L_2, also there is a minimum size constraint, L_2 is much more than $\frac{R_L}{\omega}$.

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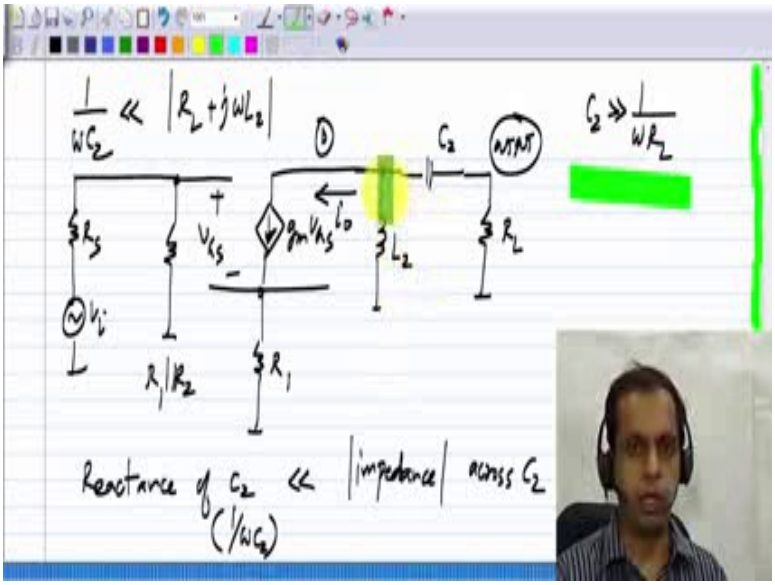

Now let see how to evaluate the constraint on C_2. How do you choose C_2, the reactance of C_2 at the signal frequencies, which is basically $\frac{1}{\omega C_2}$ must be much smaller than the impedance that appears across it, I really mean the magnitude of the impedance that appears across C_2. This is something familiar to us, we have evaluated earlier in context common source amplifier; the transfer function assuming that C_2 is short circuit and also the transfer function including C_2 and we found that if reactance of C_2 is much smaller than the resistance across it then this condition will be satisfied and you will get the same output voltage. And of course the same output current in this case whether you have C_2 for that we replace it with the short circuit.

In this case I am generalising it to impedance because across C_2, you have L_2 and a resistance R_L. Now all of this part is circuit drops out. If I deactivate v_i if I set v_i to zero, this voltage become zero and that voltage become zero, so $g_m v_{gs}$ becomes zero. So, this goes away and this is all we have left. And we can evaluate this condition it is not difficult what we want is $\frac{1}{\omega C_2} \ll ¿\, R_L + j\omega L_2 \vee ¿$. Once you have chosen L_2, you can do this. Now while discussing the output coupling capacitor in the common source amplifier, I also mention another constraint.

If this impedance, the reactance of L_2 is very large what can happen is that although this condition is satisfied, the voltage here can be quite different from voltage there, that is the voltage in drain of the MOS transistor is very different from the output voltage and that is undesirable. Because a MOS transistor is a non-linear device, and you do not want unnecessarily large voltage swings across it. You know that if you are on a non-linear characteristic the larger voltage swings you have the more the non-linearity you exercise. So, you do not want any unnecessary voltage swing at the drain node or any nodes of the circuit. This will become clearer after we discuss what are known as swing limits, the limits of signals that we can apply to non-linear devices, but for now you can take it from me that it is desirable to have the drain voltage to be as close to the output voltage as possible.

And what was the condition for that, in fact it was simpler, the condition for that was that

$C2 \gg \frac{1}{\omega R_L}$, that is the reactance of the capacitance C_2 must be much smaller than R_L, that

is C_2 must appear like a short circuit when compared to R_L, not that total impedance across it, but compared it just R_L. So that is the condition that we are going to use in this case. So, it is possible to ac couple, the output current i_o into a load resistance if we chose the reactance of L_2 to be much more than that of R_L and reactance of C_2 to be much smaller than that of R_L all of this i_o will go into R_L. The only problem with is that the inductors are usually very bulky and they are not very commonly used.

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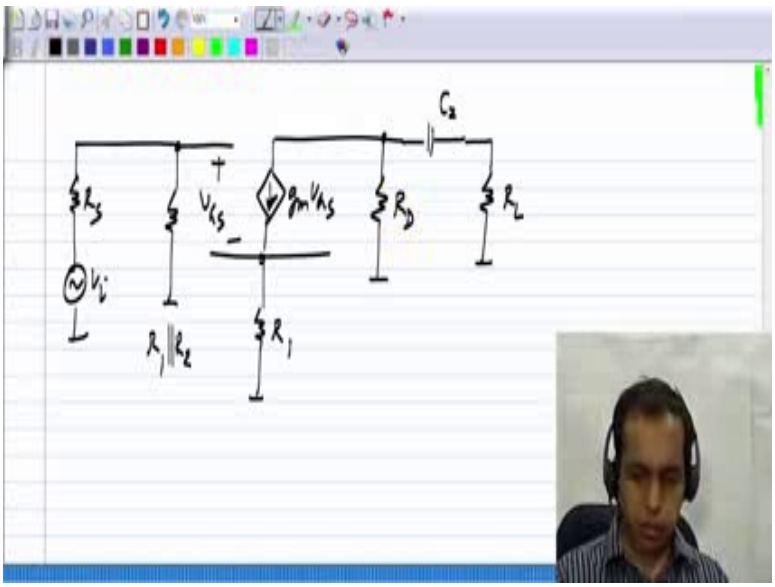

Now because inductors are very bulky and are somewhat cumbersome to use in many case you do not even use L_2 you use a resistance instead R_D. Now in the complete picture, basically this L_2 is replaced by some R_D. Now this again looks very familiar; the output part of it looks is exactly like what you had in common source amplifier. This part you have R_D here C_2 and then R_L.

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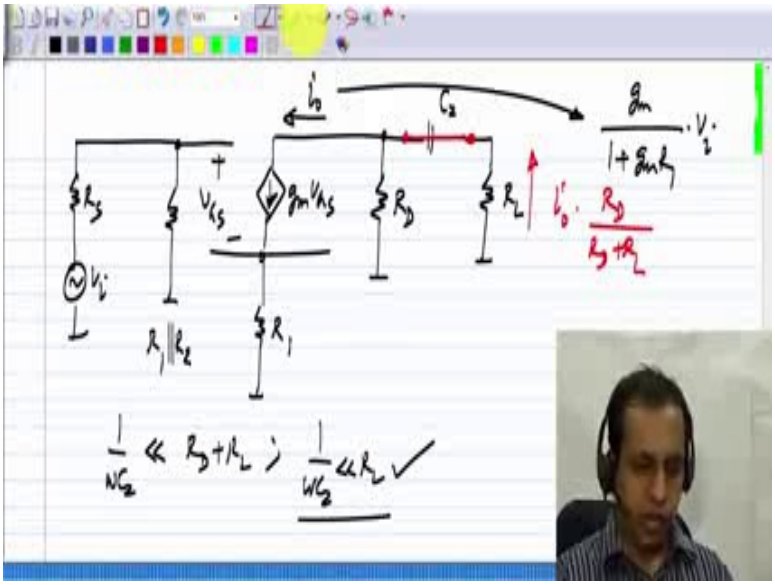

So, what are the conditions that must be satisfied by C_2, for the output voltage to be the same or the output current through R_L to be the same whether C_2 is short circuit or C_2 is there, we need the $\frac{1}{\omega C_2} \ll R_D + R_L$. But like I have mentioned many times for the drain voltage to be nearly the same as the output voltage, we would like $\frac{1}{\omega C_2} \ll R_L$. So, we will assume that we use this, in case of common source amplifier problem I asked you sometimes use this and sometimes use that, but what for now let us as we use this one. So, if that is the case C_2 becomes the short circuit.

Now what is the actual current flowing through the load, this current i_o here is the desired output of the voltage controlled current source. This is equal to $\left(\frac{g_m}{1+g_m R_1}\right) v_i$. Now clearly

not all of it flows into R_L. Assuming that C_2 is a short circuit, a part of i_o will flow into R_L and how much is that, this current will be $i_o(\frac{R_D}{R_D+R_L})$; it just the current divider formula. Now this fraction is going to be less than one, and you can just cannot help it; if you do not want to use a large inductor here, you have to use the resistor. You could try to make the resistor as large possible,

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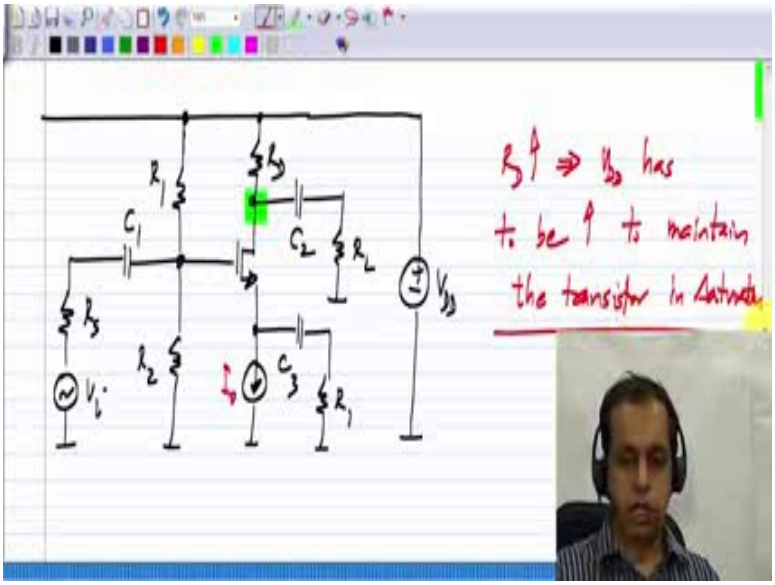

but then you will run into the same problem that you did when you made the common source amplifier. If R_D id very large, then this bias current I naught is going through R_D and to maintain a certain drain voltage which is required for saturation, the supply voltage has to increase. So, if R_D is very large, V_{DD} has to be increased to maintain the transistor in saturation region.

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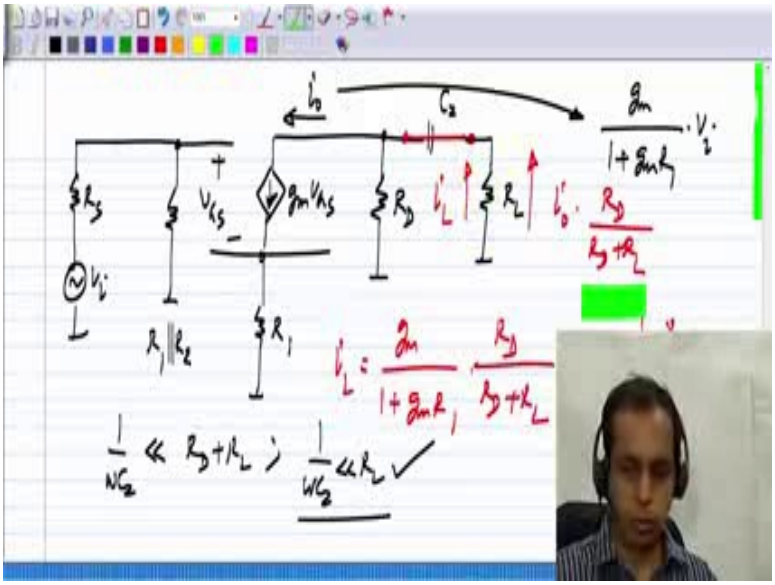

So, there is some limit to what R_D you can have, so that means, that it is only a fraction of this current that goes into R_L and that may be ok because this is still a resistor ratio we accurately determine. So, the output current, let me call this i_L,

$i_L = \left(\frac{g_m}{1+g_m R_1}\right)\left(\frac{R_D}{R_D+R_L}\right) vi \quad \left(\frac{1}{R1}\right)\left(\frac{R_D}{R_D+R_L}\right)$. So, this number is still independent of g_m of the transistor and that can be important. So, many times the voltage controlled voltage source is used in this mode.

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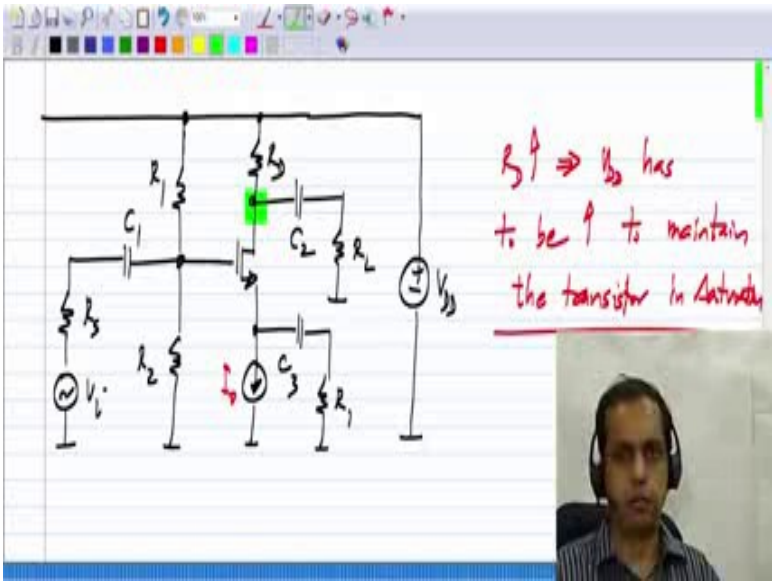

So, you have a resistance R_D and this. So this looks exactly like a common source amplifier except when we have common source amplifier we have C_3 just going to ground, now we have extra resistor R_1. So that completes the voltage controlled current source including biasing and to ac coupled current you need an inductor, but you can use a resistor and then take a penalty in the actual fraction of the current that goes to the load. And it is used like that in many occasions; this is also widely used circuit, one of the basic amplifier structures using a single transistor.