Analog Circuits
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Module - 05
Lecture – 09

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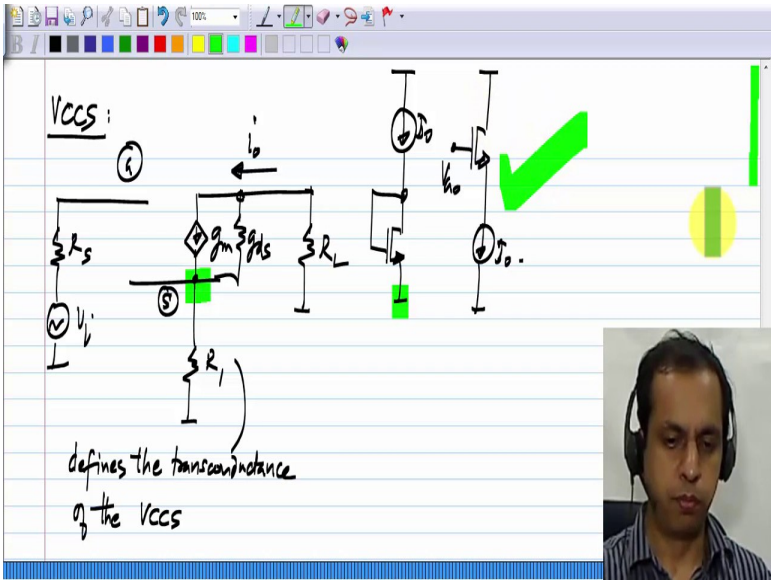

We have derived the small signal model incremental picture of the voltage controlled current source using a MOS transistor, and it looks like this. The input source represented by a series combination of v_i and R_s is applied to the gate of the MOS transistor. And from the source of the MOS transistor, a resistor R_1 is connected to the ground and this defines the trans conductance meaning the ratio of output current to input voltage of the V C C S we want to realize. And for the trans conductance to be determined only by R_1; $g_m R_1 >> 1$. And the load is connected between drain and ground, so the output current goes through the load. And of course, the MOS transistor can have an output conductance g_{ds}. Now, this is the functional incremental picture; and we have to combine it with a suitable biasing method.

There are four biasing methods available for biasing the MOS transistor at a given current depending on where you sense the difference between drain current and the desired current, and where you apply the feedback to. Just like we discussed in case of the source follower, the bias circuits involving op amp seem to elaborate and complicate for a simple circuit like this. So, we

consider the other two circuits; one of them is drain feedback, and the other one is source feedback so which of these would you like to use. Like I said earlier, it is based on convenience and just as in the case of the source follower, this appears more convenient, because the source terminal of the MOS transistor is not connected to ground in the signal picture, whereas here it is connected to ground.

Whereas, in case of source feedback in the incremental picture this i_o drops out, it becomes an open circuit and the source is floating. So, we are free to connect it wherever we want. So, this is what is more convenient and that is what we are going to use.

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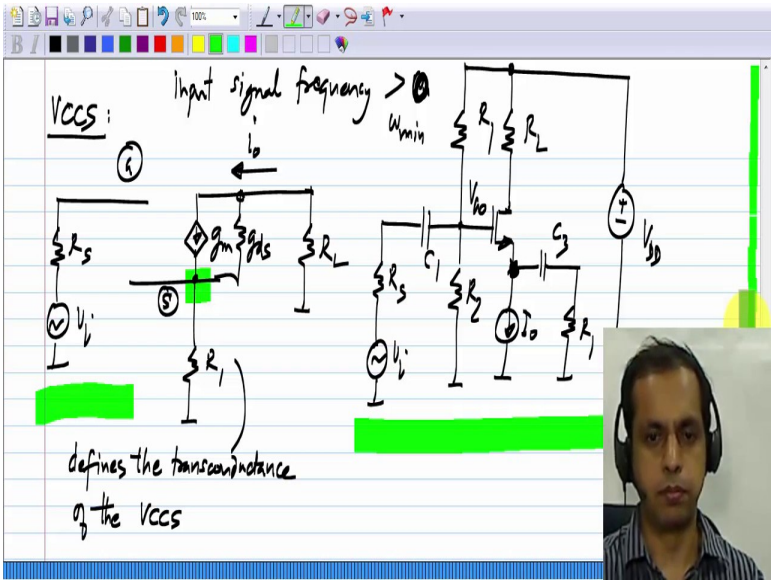

Now, how do we combine these, let me put down the bias circuit. We have a current source from the source terminal to ground; and the drain as far as biasing is concerned, it is just connected to the supply voltage – V_{DD}. The gate should be biased a fixed voltage V_{G0}; of course, we do not use another dc source for that; we use the voltage divider from V_{DD}. So this is the complete biasing picture, and it biases the transistor in saturation region, because the drain voltage is higher than the gate voltage. Now in our voltage controlled current source, we apply the input to the gate, and this is by now a very familiar scheme. As usual, I assume that the input signal frequency is greater than a certain positive ω_{min}, greater than zero. There is certain minimum frequency for the input signal. In other words, we do not have dc inputs.

In that case, what we do, to add the signal to that; we use ac coupling, through this capacitor C_1. Now this resistance R_1 must be connected between source and ground for signal frequencies. The easy way of doing that is by ac coupling that to the source terminal. In the incremental picture, I_o becomes an open circuit, because its reactance at the signal frequency is chosen to be sufficiently small. So, R_1 appears from source to ground. Now, this load resistance R_L has to go from drain to the small signal ground. There are various ways of connecting it; for now, I will assume that this is an actual resistance, so if it is actual resistance, I can simply connect it between the drain terminal and the supply voltage. The supply voltage is the small signal ground, so this R_L appears between drain and ground.

Later, we will see what to do when this R_L is not resistance per se, but it is a representation of something that comes afterwards. So, now this is the complete circuit of the voltage controlled current source. We can also see how closely it resembles the source follower circuit.

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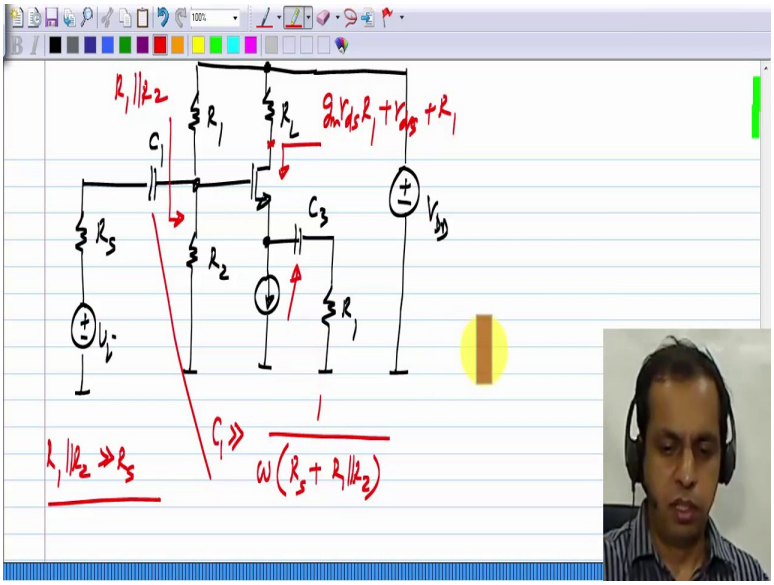

Now, the input resistance of this circuit looking in here, I am not going to write the small signal picture separately for it. This is by now very familiar picture, the input resistance is just $R_1 \parallel R_2$; no current flows into the gate, but R_1 and R_2 appears between gate and ground. But R_1 and R_2 can be chosen to be arbitrarily large, because no current flows into the gate, so you choose R_1 and R_2 such that $R_1 \parallel R_2 >> R_s$. The output resistance again we have evaluated, there is no change there;

so if we look into the drain that is between the drain and ground, we will see an incremental output resistance which is equal to $g_m r_{ds} R_1 + r_{ds} + R_1$. So, there is no change there either then we have to evaluate the constraints on the capacitor. So, this C_1, again I am not going to spend any time on it, because we have done this so many times before. The reactance of C_1 must be much smaller than what appears across it, which is $R_s + (R_1 \parallel R_2)$; this is the resistance that appears across C_1.

So, $C_1 \gg \frac{1}{\omega(R_S + R_1 \vee ¿ R_2)}$. Now what about C_3, C_3 must really be a short circuit at signal frequency, so that R_1 appears between source and ground. And this one also we have calculated before, but I will show you the calculation once more.

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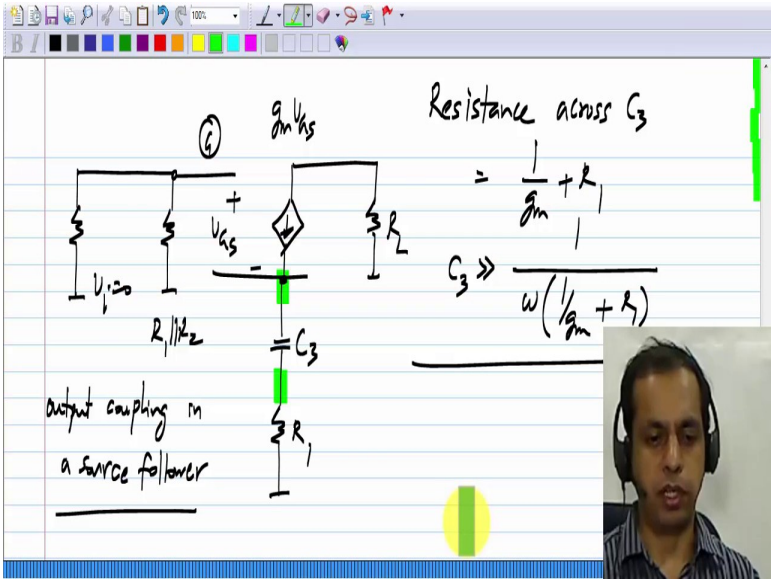

v_i is set to zero, and we have $R_1 \parallel R_2$ from the gate to ground. We have R_L, and there is capacitance C_3, and resistance R_1. We have to evaluate the resistance that appears between these two. Now I have omitted the output conductance of the MOS transistor; if you do include that the calculations become somewhat cumbersome, but they do not add any insight into the problem. As long as the output conductance is very large, the result that we derive without it are a good enough approximation. So I am going to derive it without that. Now, it turns out that we have already derived this, where did we derive this, this is for coupling the output in a source follower.

The picture looked exactly like this expect that this R_L was not there, the drain was connected directly to ground, but that makes absolutely no difference to the calculation. You can do this by yourself, you can apply a test voltage between these two, and find the resistance that appears between these two points or you can find the resistance looking up and looking down which is R_1 and add them up. The bottom line is the resistance that appears across C_3 ¿$\left(\frac{1}{g_m}\right)+R_1$. So, the reactance of C_3 has to be much smaller than this or $\frac{1}{\left(\frac{1}{g_m}\right)+R_¿}$ ¿ .

$$\omega ¿$$

$$C3 \gg \frac{1}{¿}$$

Now, this is the good enough approximation even when a large r_{ds} is present, so we are going to just use this result. So, that completes the basic discussion of the voltage controlled current source; you know how to choose g_m for a given trans conductance that we want to realize, and we also know how to combine the bias circuit with the incremental circuit.

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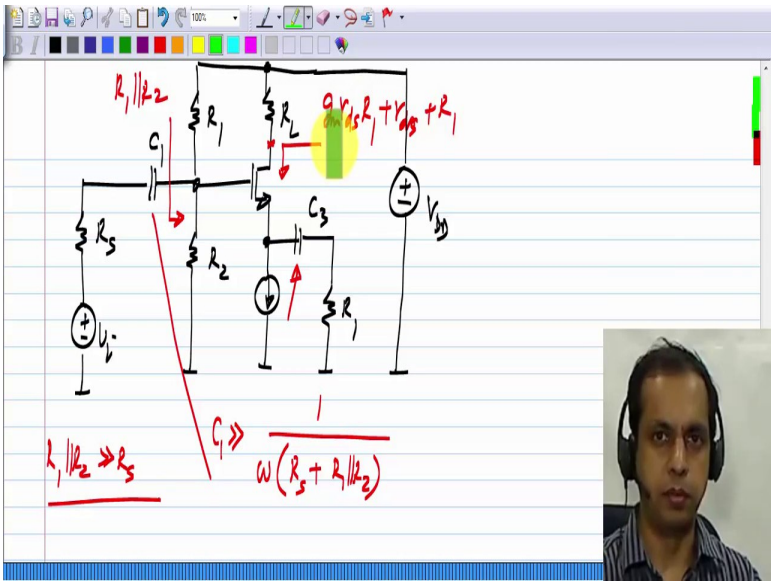

The complete circuit is shown here. In this case, I have connected the load directly between drain and V_{DD}, if that is not possible, we have to also ac couple it in some way, we will see how to do that.