Analog Circuits
Prof. Nagendra Krishnapura
Department of Electrical Engineering
Indian Institute of Technology, Madras

Module - 05
Lecture – 06

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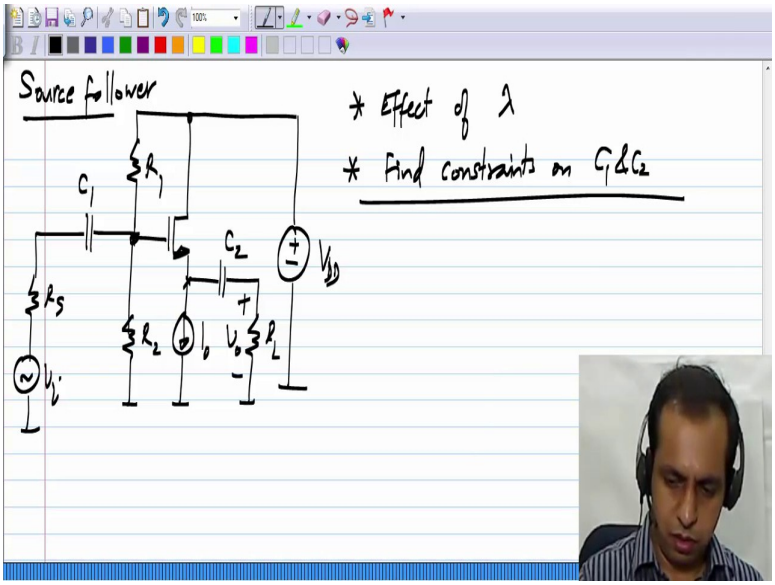

Here is the source follower that we have obtained by trying to construct a voltage controlled voltage source of gain one around a single MOS transistor using negative feedback and then adding an appropriate biasing scheme to it. We have done the analysis as well we know input resistance and the output resistance and the expression for the gain. Now, there are few small details remaining; one is the effect of channel length modulation that is non-zero output conductance of the transistor and then also to find the constraints on C_1 and C_2. So, let us take these things one by one.

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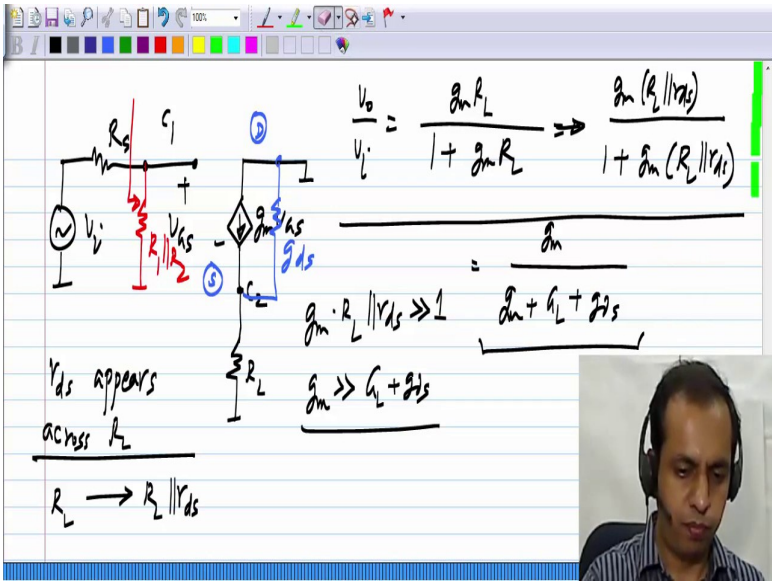

The small signal picture is this, and I will assume that the capacitors looks like short circuits at the signal frequency, C_2 would have been there. This is v_{gs}, and the current is $g_m v_{gs}$. Now, this of course, assumes that there is no output conductance for the transistor, but if there is an output conductance then it would be connected between the drain and source terminals of the MOS transistor that is where g_{ds} would be. And the effect of this is very, very easy to analyze. You can see that this g d s appears across R_L, so r_{ds} appears across R_L, so this means that in all the expressions wherever you have R_L, it should be changed to $R_L \| r_{ds}$.

This is in the expression for gain; we have $\frac{g_m R_L}{1+g_m R_L}$ for the original circuit with r_{ds} equals infinity or g_{ds} equals zero and this should be change to $\frac{L \vee ¿ r_{ds}}{R_{¿} ¿ R ¿ \frac{L \vee ¿ r_{ds}}{¿¿ ¿ 1+g_m ¿ g_m ¿ ¿}}$. Or another way of writing

it is $\frac{g_m}{g_m + G_L + g_{ds}}$. And the condition for nearly unity gain is that gm(R_L || r_{ds}) >> 1 or g_m >> G_L + g_{ds}. And it does not make any difference to the input resistance; in this case, I did not show R_1 || R_2, but whether it is there or not, the resistances looking in here is not affected by R_L in this particular case. In general, it can be in a circuit, but in this case, it is not. So, R_{in} is not affected, the gain is affected, the gain will reduce a little, because essentially you have an extra load instead of R_L, you have R_L || r_{ds}.

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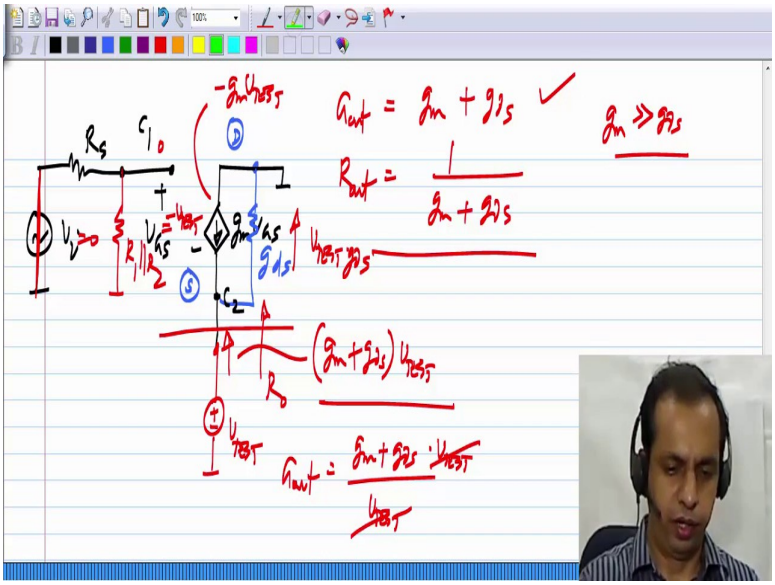

And as far as the output resistance is concerned, let me copy over this circuit. We compute the output resistance looking that way. And v_i is set to zero; that means, this becomes a short circuit, and this is very easy to compute. First of all, you can notice that this g_{ds} simply appears between the output terminal and ground, so whatever output conductance we have calculated earlier which was equal to g_m, now you will have an additional g_{ds}, but we can also evaluate it and see, if I apply V_{TEST} here, the gate voltage is at zero, because this is zero, and no current flows into the gate, and the source voltage is at V_{TEST}, so v_{gs}=-V_{TEST}, so this current source here is - $g_m V_{TEST}$. And the total current going in here is the current in this going upwards plus the current in that going upwards and the current in this going upwards is $V_{TEST} g_{ds}$, so this total current will be - $g_m V_{TEST}$ is simply $g_m V_{TEST}$ going upwards, so the total current is $(g_m+g_{ds})V_{TEST}$. .

So, the output conductance is the current divided by voltage, and; obviously, this gives you g_m+g_{ds}, or if you want the output resistance it is $\frac{1}{g_m+g_{ds}}$. Now, g_m is likely to be much more than g_{ds}, when you bias the transistor in saturation region. So, this does not change the output resistance by much, it reduces it only by a little bit.

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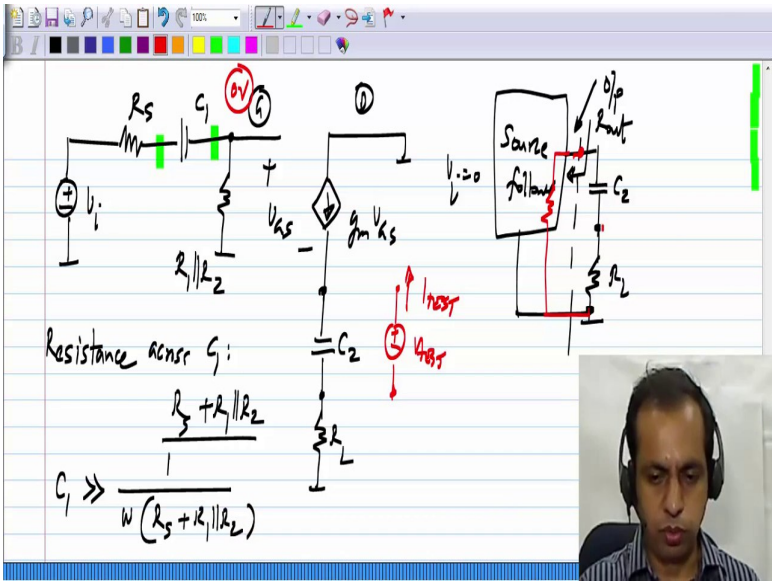

Now, I will draw the small signal equivalent including the capacitors, so that you can find the constraints on them. Here is the input voltage, R_s, C_1 and we will have $R_1 \parallel R_2$ between the gate terminal and ground. The drain is connected to the ground, and this is connected through a capacitor C_2 to R_L. This is $g_m v_{gs}$, where v_{gs} appears here. Now, the input side of this is very, very familiar right. If you set v_i to zero, what is the resistance that appears across C_1, we have calculated this many, many times, so the resistance across C_1, this is basically $R_s + R_1 \parallel R_2$.

So, the constraint on C_1 is that it should be much greater $\frac{1}{\omega\left(R_s+R_1 \vee R_2\right)}$.

As usual while calculating C_1, your short circuit C_2, but I mean in this case, it does not matter, because the value of C_2 does not affect the value of C_1 anyhow. The circuit is truly decoupled. Now, as far as calculating C_2 is concerned, we set the input to zero, and because the input is zero, and no current flows into the gate, you can easily work out that this voltage is at zero. This is true whether we have C_1 that is very large or not. So, this will be at zero. Now, you

have to find the resistance that appears across C_2. How do you do that, there are couple of ways of doing it, I will choose the easy way. You can of course, connect a voltage source V_{TEST}, and it has to be connected remember between this terminal and that terminal and calculate the current flowing I test, and take the ratio.

Now, we have already done part of the calculation right, because this picture, it is looks like this. We have C 2 and R L connected to ground and it is going into the output of this source follower, which is also connected to ground and this is the output terminal. Now, we know that when the input is set to zero, looking back in here, what do we see, we see the output resistance of the source follower. In fact, we use this method also for the common source amplifier with drain feedback. So, you see the output resistance of the source follower. And if I write that here show it as resistance between that point and ground and this is what we will have.

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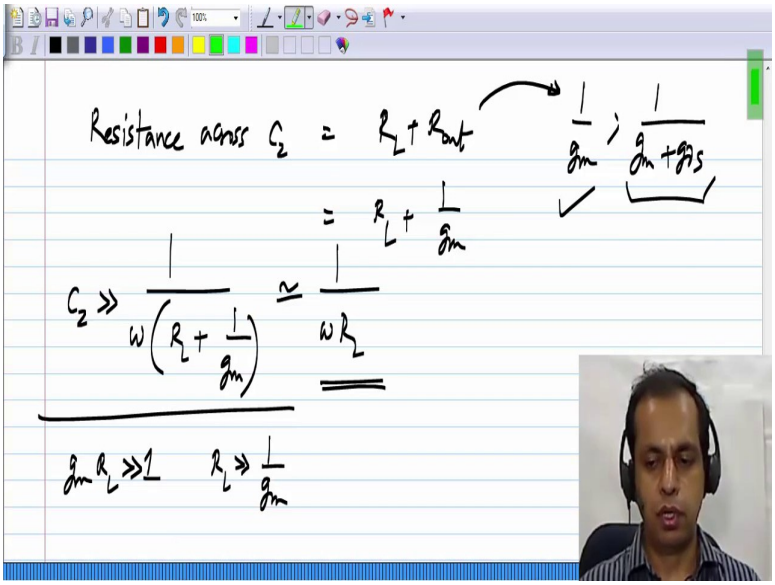

So, what is the resistance that appears across C_2, you clearly see that it is R_L plus the output resistance of the source follower. And the output resistance of the source follower is $\frac{1}{g_m}$ if you neglect g_{ds} or $\frac{1}{g_m + g_{ds}}$; just for simplicity I will use this expression, but you can also use this, it is anyway not going to be much different from that one. So, this is equal to R_L+

$\frac{1}{gm}$. So, what is the constraint on C_2, the reactance of C_2 must be much smaller than the resistance that appears across it. So, C_2 has to be much more than $\frac{1}{\omega\left(R_L+\left(\frac{1}{g_m}\right)\right)}$. And for a source follower to behave like a source follower, like a unity gain buffer, anyway you need $g_mR_L >> 1$, so this means that $R_L >> \frac{1}{gm}$. So, these constraints approximately is that it is $\frac{1}{\omega R_L}$.

So, again quite easy to compute, and it is computed in a way that is similar to what we have done many times before. And just for practice, I would encourage you to actually connect the test source between these two terminals and find the current that will give some extra practice in circuit analysis. And of course, you should get exactly the same answer that I got.

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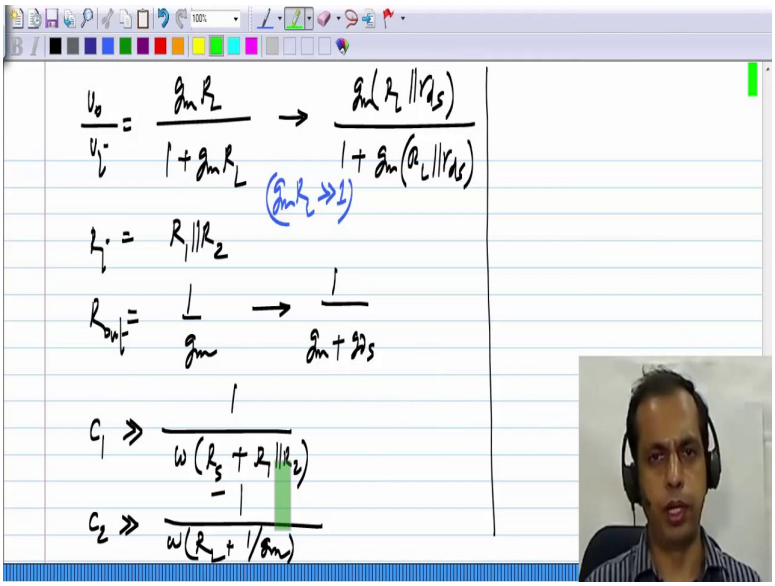

So, now we have everything that we want to know if we want to design a source follower, the gain of that is $\frac{g_m R_L}{1+g_m R_L}$ or if you want to include g_{ds}, $L \vee ¿ r_{ds}$ $R_¿$ ¿ R ¿ $L \vee ¿ r_{ds}$ ¿¿ ¿ $1+g_m ¿$ $g_m ¿$ ¿ . By the way notice that I use the conductance form of the resistance form depending on whichever is convenient, you should also get used to it, because that is quite commonly done in circuits. And the input resistance is really due to the biasing resistances, the output resistance is $\frac{1}{g_m}$ or $\frac{1}{g_m+g_{ds}}$. And the capacitors have these constraints that is the constraints for C_1, where R_s is the resistance of the driving source and C_2 has to be much more than $\frac{1}{\omega\left(R_L+\left(\frac{1}{g_m}\right)\right)}$.

So, with this, you should be able to design a useful source follower given the value of R_s and R_L; given the value of R_L, you choose g_m such that $g_m R_L >> 1$, that is necessary. And given the value of R_s, you choose R_1 and R_2 such that the combination $R_1 || R_2 >> R_s$, so that way there is no attenuation and you get a nice unity gain buffer.