Analog Circuits
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Module - 05
Lecture – 05

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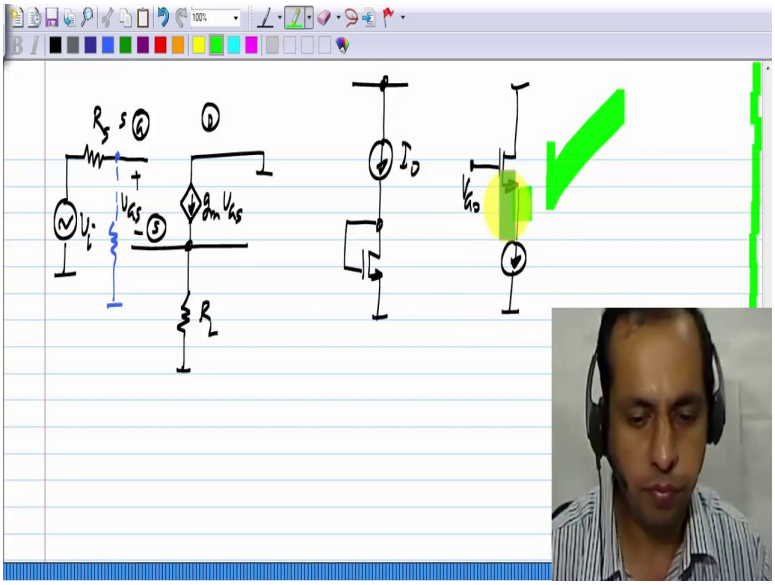

Now, I will combine the small signal picture of the voltage controlled voltage source or source follower which we have synthesized with a suitable biasing arrangement to complete the circuit. Now, the incremental picture looks like this; drain, gate and source of the transistor. This is of course, v_{gs} and the load is connected there. Now, we know from our experience with common source amplifier that when we setup the biasing arrangement for the transistor, there could be some extra components. For instance, to bias the gate, there could be some resistors and so on so that may also happen then we will have to put the constraint on their values so that we still have the result that we wish to have.

Now, what is the suitable way of biasing the MOS transistor; there are first of all four different ways. The drain feedback bias, the source feedback bias; and sensing at the drain, feeding back to the source; and sensing at the source, feeding back to the gate; out of these four, the last two of them and sensing at the drain, feeding back to the source; or sensing at the source, feeding back to the gate involve yet another inverting amplifier stage. I illustrated

these circuits with an op amp, but there is some extra amplification state that is required so that you have the inverting gain from drain to source or source to gate.

Now, that for now it is just too complicated, because after all we are looking at a single transistor circuit, and we do not want just for biasing to use another op amp. We prefer not to use such complicated biasing arrangements in this case. The remaining two are drain feedback where we have a current source connected to the drain, and drain is also connected to the gate for feedback. And source feedback where a current source is connected to the source terminal. And the gate is connected to a fixed voltage. So, how would you choose between the two, you choose based on which is more convenient. The first thing you notice is that in this circuit here, in our circuit the source terminal is not connected to ground whereas, in the common source amplifier it was connected to ground.

So, if we use this first circuit, the drain feedback circuit, the source is connected to ground or it could be connected to a fixed voltage, but in the incremental picture this will be ground. So, somehow if we use this, it has to be connected to ground for the biasing arrangement, but it has to be lifted from ground for small incremental purposes that can be done using an inductor and so on, but it is again cumbersome. Whereas this second circuit, the way it is the source is anyway not connected to ground, which is how we want it here. In the incremental picture, the current source becomes an open circuit, and the source is floating as it is right that is exactly what we want here. So, this is the most convenient circuit for use with the source follower or the common drain amplifier so that is what we are going to use.

Now, it is possible to combine any incremental picture with any biasing circuits using a proper combination of capacitors and inductors, but some of them will become too cumbersome, because our goal is not just to realize circuits that work, but also do them in the most efficient way possible. Now, it does not mean there is always one unique choice, but in this case at least the second one appears more convenient and let us use that one.

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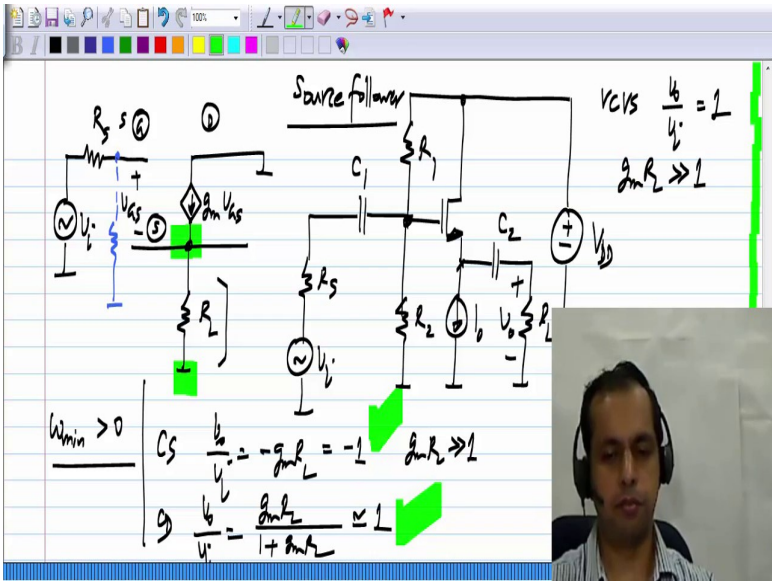

So, let me redraw the biasing part; let say it is biased to the current I_0. The drain it is connected to the incremental ground here, but it cannot be connected to ground over there, because then we cannot have the transistor in saturation, the drain voltage has to be above the source voltage. So, let say that it is connected to some fixed voltage and that is nothing, but the supply voltage V_{DD}. Remember this is what we did when we came up with the biasing circuit in any case. The gate has to be connected to the fixed voltage and as before we do not want to use yet another dc source for biasing the gate. So, what do we, we take the drain voltage, divided appropriately using a resistive divider and bias the gate.

And this is the perfectly acceptable arrangement, because the gate draws no current, so the values of R_1 and R_2 can be arbitrarily set. If you look at this voltage, it will just be $\left(\frac{R_2}{R_1+R_2}\right)V_{DD}$, whether you connect the gate or not, because the gate does not draw any current. So, now we have a transistor that is bias the current I_o and it is in saturation and so on. Now, we have to somehow connect the input source to it, and the load to it. Now, we have done this so many times, it is quite easy. I am sure you can do this with your eyes closed. We have the signal source v_i, now how do I connected to this, again I will use the constraint that I have been using for all the circuits so far. The minimum signal frequency is greater than zero that is we are not interested in a dc signal. It has some minimum frequency; it could be one kilo hertz, it could be one hertz, it could be one megahertz, whatever it is, but it is not zero.

In that case, we can use capacitive coupling to combine, the dc value obtained from the voltage divider with the signal obtained from the source. So, I do this, and this picture now must look very familiar to you. And how do I connect the load, the load must appear between the source terminal and ground, so I ac couple it, because first of all this is not just a resistance as I have repeatedly emphasized, it is just the representation of what comes later. But even if it were just a resistance, if you connect it there, what happens is, there will be some voltage here, and some current drawn by this, and the current through the MOS transistor will not be just I naught, it will be I naught plus the current through the resistor. So, the bias will be disturbed, so we do not want that.

So, the correct way to connect the load resistance R_L is by ac coupling through a capacitor C_2 so that is all that is there to it. Now, we have bias the transistor, we have connected the input and we have also taken the output. So, this circuit is the complete diagram of the source follower or the common drain amplifier or a voltage controlled voltage source with gain of approximately one. Now, we have to choose the current I_o such that $g_mR_L >> 1$, the output of course, is here. It is quite common to show this as one of the elementary stages using a MOS transistor, you show the common source amplifier and then the common drain amplifier and so on. But we prefer to think of it as the feedback arrangement, because feedback is essential

to making the gain of this stage $\frac{v_o}{v_i}=1$.

Now, the important thing here is this is quite different from a common source amplifier

whose gain is $-g_mR_L$. You can always set $R_L=\frac{1}{g_m}$, and make this equal to - 1. But what

happens is if the value of R_L changes, if we choose a different load resistance, the gain will change. Similarly, if temperature g_m will change and the gain will change. Whereas, in our

source follower or the common drain amplifier, $\frac{v_o}{v_i}=\frac{g_m}{1+g_mR_L}$. And we choose $g_mR_L >> 1$.

Now, clearly you can see that if R_L changes a little bit as long as you satisfy this condition, the gain will be one, the gain will be close to one. The exact value of R_L does not matter. If

$g_mR_L >> 1$ in the denominator, 1 is negligible compared to g_mR_L and this gain will be close to 1.

Also if because of temperature and so on, if g_m changes a little bit, again nothing happens, because this $g_mR_L >> 1$ and the gain will be close to 1. So, there is a qualitative difference between the common source amplifier, which has no feedback and a common drain amplifier which has feedback. The circuit with feedback, the common drain amplifier is much less sensitive to the load and source conditions as well as the operating point and the small signal parameters of the MOS transistor. So, this is a very important distinction.

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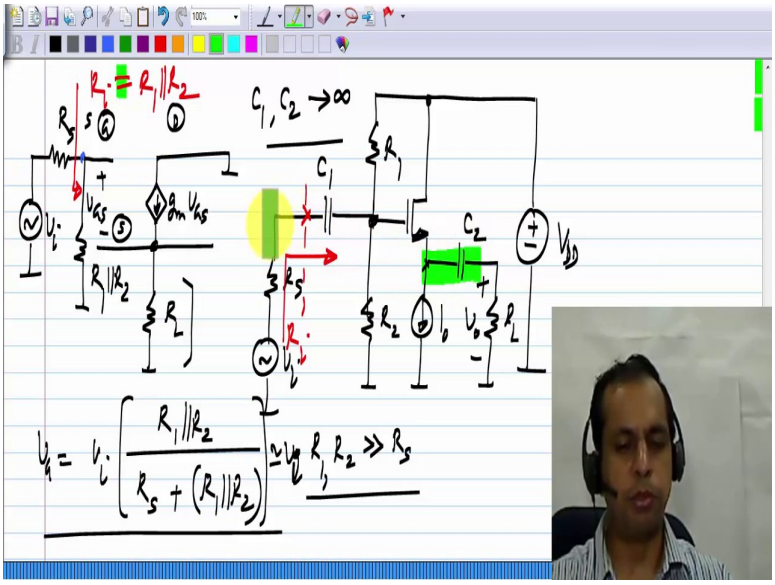

Here, I have put down the small signal picture of the source follower that we originally synthesized, and the complete circuit diagram that we got by trying to combine this with a suitable biasing arrangements. Now, what is the difference between this and this; this circuit is not complete, because R_1 and R_2 are missing from the picture. $R_1 \| R_2$ must appear here. They go from gate to V_{DD}, which is the same as small signal ground and also they go from gate to ground. So, $R_1 \| R_2$ appears between gate and ground so that is all that is there to it. So, this is now the complete small signal picture corresponding to this circuit with the assumption that C_1 and C_2 are large enough so that they are shorts. They are very large that is the assumption.

So, what is the essential difference and functionality, the only thing is there is now a voltage division between the actual input source v_i and the gate terminal of the MOS transistor. We

wanted the input resistance of the source follower that is here, wherever you connect the source right, looking in there we wanted that to be infinite. Now, we know that it is not infinite. What is it, I am not going to evaluate this separately, it is very easy to see that it is equal to $R_1 \parallel R_2$. So, now the gate voltage is not exactly the same as v_i. The gate voltage will be $v_i\left(\frac{R_1 \vee ¿ R_2}{R_S + R_1 \vee ¿ R_2}\right)$. In fact, we had got exactly the same type of expression with the common source amplifier as well, when we use this type of biasing, the source feedback biasing, but this situation is quite easy to take care off. You have to make sure that both R_1, $R_2 >> R_s$. If you do that then this ratio will be very close to one, and the gate voltage will be approximately equal to the input voltage, so that is the only thing that is come about because of the biasing arrangement. Everything else looks exactly like this right, R_L is connected to the source, and it will be connected the source if C_2 is sufficiently large, is it fine?

So, this completes the circuit of the source follower or the common drain amplifier, and it is a quite useful circuit, it is used in a lot of places. For instance, the microphone into which I am speaking; many of them microphone itself will have a very high output resistance or very high value of R_s. And it would not be able to drive the following circuit, so it is very common to use a source follower immediately following the microphone so that you have the same signal here as that comes out of the microphone, but the output resistance is much smaller. So, this can drive a much heavier load and consequently not attenuate the signal from the microphone. So, it is a very widely used circuit and it is one of the basic amplifier topologies; the common source is the other one.