Analog Circuits
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Module - 05
Lecture – 04

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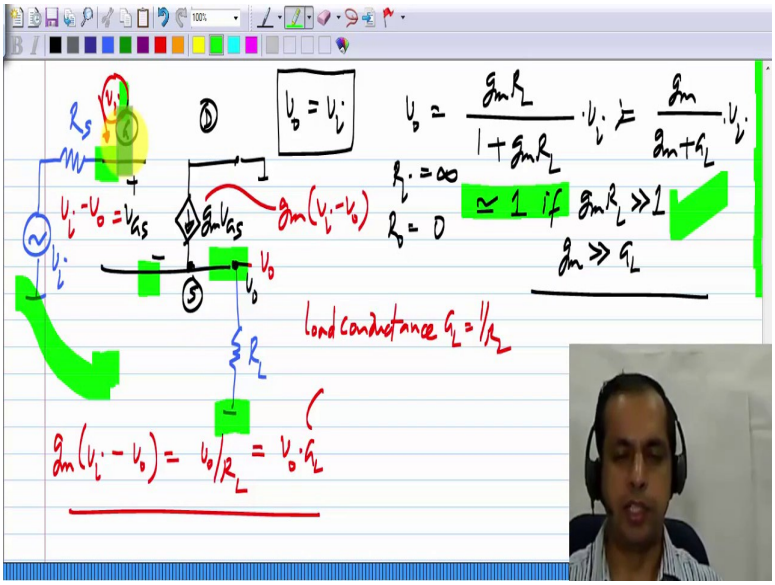

Using the principles of the negative feedback, we have come up with the topology for a voltage controlled voltage source with a gain of one using a single MOS transistor. Now, let us analyze it further. This is the small signal picture of a MOS transistor, and as is quite common while doing preliminary analysis of circuit, I have ignored the output conductance. Now, we said that the input voltage must be applied to the gate terminal, the output must be taken from the source terminal and the drain terminal is grounded. When I say the input is applied to the gate terminal; obviously, it means between the gate and some common ground to which the drain is also connected. And similarly, when I say the output is taken from the source terminal, it means between source terminal and ground.

So, let me put those things down as well. So, I have a source v_i, and it usually has some non-zero resistance R_s and that is connected between the gate and ground. The output, it is taken between source and ground, what it means is that I connect the load resistance here, both this source that is the voltage source in series with the resistance and the load which is just the resistance are representations of what comes before and after. It may not really be voltage

source in series with the resistance, it represents the Thevenin equivalent of whatever is driving this. Similarly, this represents the equivalent input resistance of whatever comes after that.

So, now let us analyze this. Earlier, we kind of did some hand waving analysis and said that $v_o = v_i$. Now, of course, at the time, we did not consider the load and so on. We just said that if nothing was here then this current here would be flowing into the parasitic capacitor and steady state will be reached when the current becomes equal to zero, so the source voltage has to become equal to the gate voltage. Now, let us analyze this circuit properly and then see. It is very easy, extremely simple circuit. Now, one thing you have to be careful, when you go to different types of circuit is that in the common source amplifier the source is at ground. So, the gate voltage itself is the gate source voltage, this is of course, not true of all circuits in general.

In this case, clearly the source is not connected to ground, so do not just look at the gate voltage and assume that it is the gate source voltage.We have to take the difference between this and that to compute the gate source voltage. Now, this is the very commonly made mistake that is why I am highlighting this; many times in circuit like this where the source is not connected to ground, students tend to compute the gate voltage and multiply the gate voltage with g m to get this current source instead of actually computing the gate source voltage. Please be careful about that.

Now, this is really a one node circuit. First of all, no current is flowing into the gate, so the voltage at the gate is v_i. Of course, voltage is always defined between two terminals, so when I say voltage at some node, obviously, the other node is the common ground of the circuit. So, this is v_i. Now, the voltage at the source is the output voltage that is where we take the output from – v_o. So, what is v_{gs}, $v_{gs}=v_i-v_o$. And this current source here is $g_m(v_i-v_o)$. So, all this is known, the only thing is to equate this current to that current. There is really only one node in the circuit, where we write Kirchhoff's current law. And we have to write $g_m(v_i-v_o)=$

$\frac{v_o}{R_L}$ and sometimes it convenient to write it as v_oG_L, where G_L is the load conductance.

Extremely simple, from this you solve for the output voltage v_o and what you get, you will get $v_o = \left(\frac{g_m R_L}{(1 + g_m R_L)} \right) v_i$ or in terms of conductance $\left(\frac{g_m}{g_m + G_L} \right) v_i$. Now, what is it that we really wanted, we wanted a voltage controlled voltage source of gain one, $v_o = v_i$. Now, we have got something different, can this be equal to one, or at least close to one; of course, it can, it is very easy to see that. If $g_m R_L >> 1$, then this is approximately equal to 1. So, this number is approximately equal to 1 if $g_m R_L >> 1$ or in terms of conductances is $g_m >> G_L$. So, this also tells you how to choose the operating point of the MOS transistor. If you have a certain load resistance, you have to choose the operating point of the MOS transistor such that the g_m at the operating point times the load resistance is much more than one, or put this way the g m of the MOS transistor, the transconductance of the MOS transistor at the operating point is much more than the load conductance. If you satisfied that condition then v_o approximately equals v_i.

So, now it looks like what we got intuitively from negative feedback, does operate more or less like that, that is more or less like a voltage controlled voltage source of gain one when you connect a real source and load to it. In this case, we have connected a source with some source resistance R_s and a load with some load resistance R_L; it does behave like that. Of course, you have to satisfy this condition. Now, the other interesting characteristics of voltage controlled voltage source are the input resistance, which must ideally be infinite and the output resistance, which must ideally be zero.

Let us compute those things as well. The input resistance is evaluated between the terminals where you apply the input between the gate and ground. Remember between these two terminals is where you connect the input source. And the output resistance is computed between the source terminal and ground that is wherever you connect R_L. As I mentioned before while evaluating the input resistance, the load must be in place. And similarly, while evaluating the output resistance, the source resistance must be in place. So, let us compute these things and see what we get.

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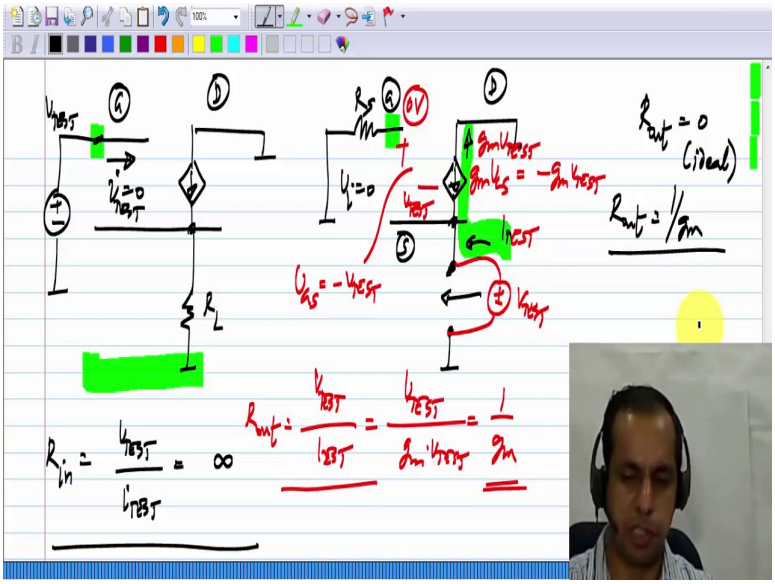

The input resistance is really trivial, but I am going to show it anyway, the drain in grounded, the gate is where you connect the input source, and the load is connected there. And what you have to do is calculate the resistance between this point and ground. Now, of course, normally what you do is apply a test voltage, find the current and so on, but it is very obvious that the current going in here is zero. So, whatever test voltage you apply between these two terminals, the current will be zero; so the input resistance which his V_{TEST} by I_{TEST}. If I do apply a V_{TEST}, I could have applied it here; I could have applied it there; $\frac{V_{TEST}}{I_{TEST}}$ is simply infinite.

So, this topology at least the way we have drawn with just the small signal equivalent of the MOS transistor, does give you the ideal value of the input resistance. The ideal value should have been infinite and it is really infinite, it is not drawing any current. And this is great, why is that, because regardless of how bad this voltage sources is, that is driving the input, R_s could be very large, but still all of these v_i appears at the input terminal, the gate terminal of the circuit. Now, what about the output resistance to calculate the output resistance, you null the input source you have v_i equals zero. And you have R_s over there, and between these two terminals is where you connect the load resistance. So, you have to find the resistance between these two terminals. The drain is of course, grounded. So, I repeat the earlier

warning please be careful about what is the source voltages and all these calculations that you carry out.

So, I will apply V_{TEST} here, and find the current flowing I_{TEST} and $\frac{V_{TEST}}{I_{TEST}}$ will give me, the output resistance. How do I go about the calculation, first of all what is the gate voltage, there is no gate current flowing, so no current through R_s, so consequently the gate source voltage is at zero volts with respect to ground. Now, what is the voltage at the source, that is equal to V_{TEST}, because V_{TEST} is connected between the source and ground. So, what is the gate source voltage v_{gs} of the MOS transistor, $v_{gs} = -V_{TEST}$, 0 - V_{TEST}. And this current source here, inside the MOS transistor is $g_m v_{gs}$, which is equal to - $g_m V_{TEST}$. It really means the current of g m V TEST is flowing upwards; minus g m V TEST is flowing downwards; $g_m V_{TEST}$ is flowing upwards. And that is exactly equal to I_{TEST}, I_{TEST} is simply $\frac{V_{TEST}}{I_{TEST}}$.

So, $R_{out} = \frac{V_{TEST}}{I_{TEST}} = \frac{V_{TEST}}{g_m V_{TEST}} = \frac{1}{g_m}$. So, the output resistance of this circuit is $\frac{1}{g_m}$, it is not zero. We wanted output resistance to be equal zero, ideally. Now, what we are getting is $\frac{1}{g_m}$. Now, we said that in a voltage controlled voltage source, the output resistance must be small; now what is it for small or large compared to the load resistance, so the output resistance must be much smaller than the load resistance.

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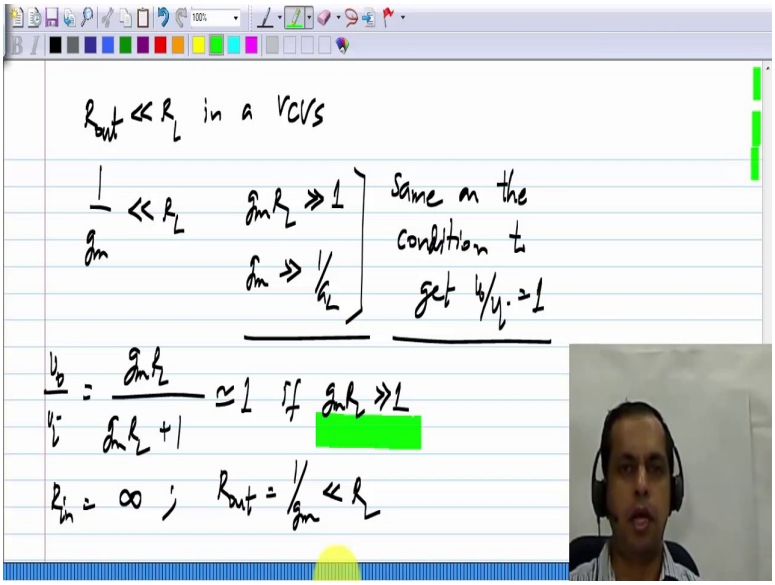

What does it mean for as in our case one over g m which is the output resistance must be much smaller the R_L. In other words, $g_m R_L >> 1$, or $g_m >> G_L$. Remember this is exactly the same condition that we needed to have the gain of the circuit, $\frac{v_o}{v_i}$ to be close to one. So, if you satisfy that you will automatically satisfy this. So, this circuit does behave like a good voltage controlled voltage source; it has a gain, which is $\left(\frac{g_m R_L}{(1+g_m R_L)}\right)$ ~ 1 if $g_m R_L >> 1$.

And R_{in} indeed infinity, and $R_{out} = \frac{1}{g_m}$ which if you do satisfy this condition, it will be much smaller than R_L. So, what we have got is the viable voltage controlled voltage source of gain one.

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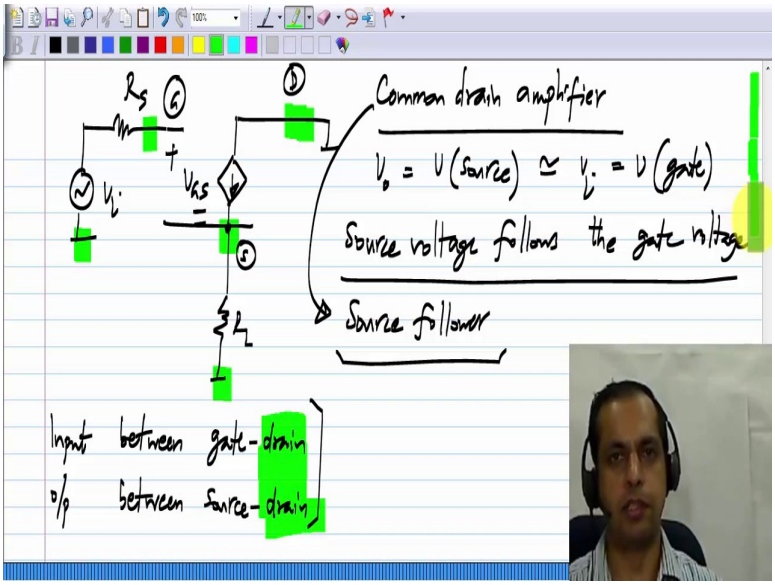

Now, in this particular circuit, we have the input, which is applied to the gate. It is applied between the gate and ground. And we have the MOS transistor, the drain is connected to ground, and the load is connected between the source terminal and ground. So, if you observe, the input is connected between gate and ground and you can also think of about it as gate and drain. And similarly, the output is taken between source and ground, or in other words, between source and drain. In a common source amplifier, the input was applied between gate and source and the output was applied between drain and source. The source was common to input and output that is why it is called the common source amplifier. And in this case, the drain is common to input and output, so this particular topology, the voltage controlled voltage source of gain one is also known as common drain amplifier. Now, there is another name for it and that comes from we know that the output voltage, which is the same as the voltage at the source terminal is approximately equal to the input voltage which is also the voltage at the gate terminal.

Essentially, the source voltage follows the gate voltage. So, for this reason, it is also, in fact, more commonly called the source follower; this means that the source voltage follows the gate voltage. So, if you see the literature, you will frequently see the terms source follower, so that is refer that refers to the common drain amplifier or the voltage controlled voltage source of gain one, so that is complete the small signal picture and analysis of the voltage controlled voltage source of gain one or common drain amplifier or source follower, whichever way you think about it. Now, what we will do next is to find a suitable biasing

arrangement for this and complete the circuit, because so far what we have is just the incremental picture that cannot be realized as it is right. The operating point of the MOS transistor has to be setup and at that operating point, the incremental picture should look like this.