Analog Circuits
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Module - 05
Lecture – 03

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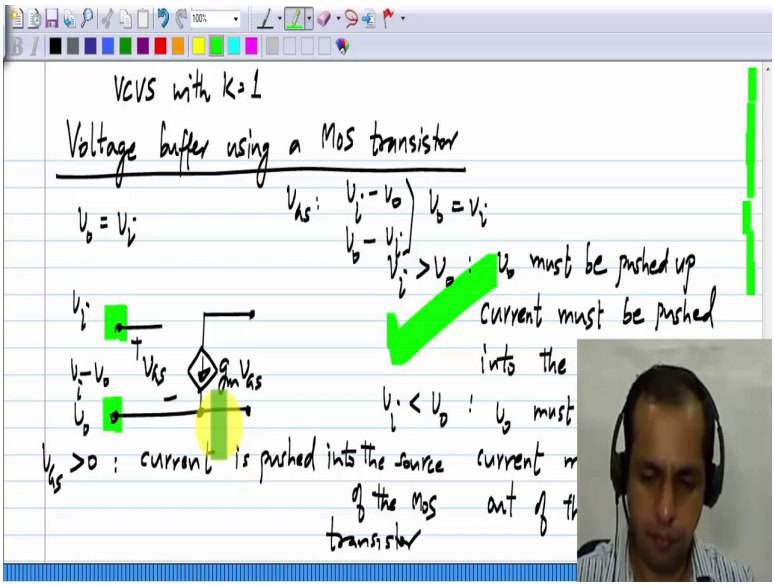

Now, we will discuss how to realize a voltage controlled voltage source with gain one or a voltage buffer using a MOS transistor. The output voltage should be equal to the input voltage. Now, a MOS transistor looks like this. And what we are thinking of is to use just a single MOS transistor to realize this voltage buffer, or a voltage controlled voltage source. Now, MOS transistor compares a gate voltage to the source voltage that is it takes the gate source voltage and multiplies it by certain constant g m to produce the drain current. So, the current depends on how much the gate voltage is in comparison with the source voltage. So, we can think of it as comparing the gate voltage to the source voltage. Now, what do we want from a voltage buffer, $v_o=v_i$.

Now, if $v_i > v_o$ then v_o must be pushed up, it must be increased. And how you do that how do you increase the voltage, this means that current must be pushed into the output node. And of course, if $v_i < v_o$ exactly the opposite must happen; v_o must be pulled down or current must be pulled out of the output node. Now, what really happens in a MOS transistor, if $V_{GS} > 0$ then this current flows from drain to source, and you can see that the current is pushed into the source node. And similarly, $V_{GS} < 0$, current is pulled out of the source node.

So, how can we arrange these voltages so that this action happens, remember v_o is the output voltage, so output voltage must be part of the comparison. What I mean is we are comparing the input voltage to the output voltage. So, v_{gs} must be either $v_i - v_o$ or $v_o - v_i$, any of these things is possible. v_{gs} is comparing the gate voltage to the source voltage, so it must be whatever we want to compare, it could be $v_i - v_o$ or $v_o - v_i$. When $v_i - v_o > 0$, then current must be pushed into the output node. And here you see that if $v_{gs} > 0$, current is pushed into the source of the MOS transistor.

You can try out different combinations, but it appears like if we apply the input voltage here, if you think of the source node as the output then what gets applied as gate source voltage is nothing, but $v_i - v_o$, and also if $v_i - v_o > 0$ then this current is flowing downward into the source node, and its pushing up the source voltage. It is pushing a current into the source node and it increases the source voltage and it is exactly the condition that you want. So, this is how we use the transistor in negative feedback. Now, I already knew what the topology must look like, so I considered only this combination, but you can try the other way around now I took the output from the source. So, instead of that you could try taking it from the drain node then you will find that you cannot arrange this negative feedback in a convenient way. You would not be able to do it.

So, when you synthesize the new circuit, sometimes you go through different choices which may be incorrect, but finally, you arrive at the correct one. So, the principle here is negative feedback, and if $v_i > v_o$, v_o must be increased; and if $v_i < v_o$, it must be pulled down and so on. And how do we increase or decrease the voltage while using a current source, we have to push current into a node to increase its voltage, and pull current out of a node to reduce its voltage.

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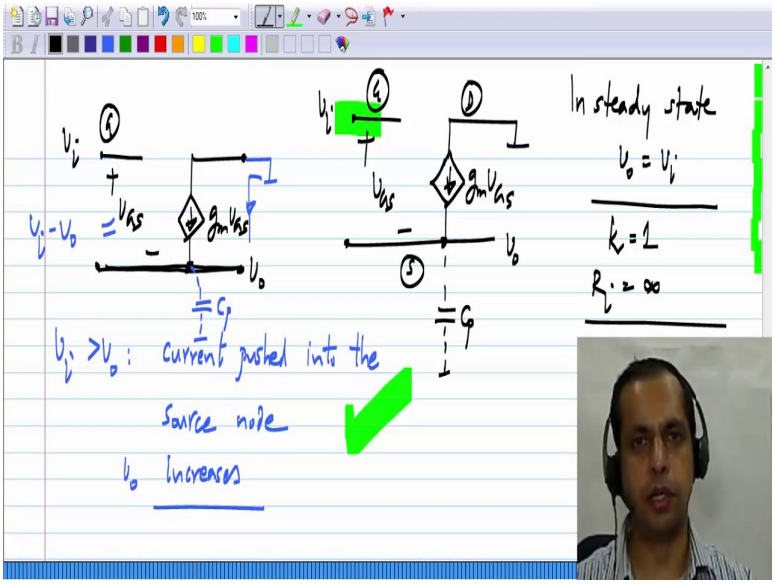

So, let me redraw this. By the way I starting from the small signal picture of the transistor, so when we want to realize the functionality such as the voltage controlled voltage source, we want to realize some functionality which is a linear function, $v_o=kv_i$ or $v_o=v_i$ and so on. So, that we synthesize using the small signal picture of the MOS transistor. Now, we know number of ways of biasing the transistor, and we can choose any one of them to go with the functional small signal equivalent circuit to come up with the complete circuit. So, in every one of these cases, the functional synthesize is done in the small signal domain, the incremental domain and you had an appropriate biasing arrangements. You will find that some types of biasing arrangements are more convenient than others, and you use the more convenient one.

So, again what I did was apply the input to the gate, and the source node here, this will be the output voltage. If I do that; obviously, the gate source voltage will be equal to v_i - v_o; we knew that between the gate and source we have to have either v_i - v_o or v_o – v_i so that we effectively comparing the input and output voltages. So, in this case, it is v_i - v_o. Now, we already designated this source as the output node, and let see if it will be consistent. Now, the drain I am not connected anywhere, so let me connect it to the small signal ground. Now, what happens if $v_i > v_o$, that is v_o is smaller than what is required, what is desired. $v_i > v_o$, then current flows this way.

And as before, remember at the source there is only the current source, so you may be wondering how Kirchhoff's current law is satisfied, but as with other negative feedback circuits, you imagine a parasitic capacitor here, and this can be arbitrarily small, it does not matter how much it is. The point is if current is pushed into this node, it goes into the capacitor and v_o gradually increases. And it is exactly what you want, because here in this case v_o is smaller than what is required, so it will be increased. And exactly the opposite will happen, if $v_i < v_o$, then v_o is too high, and this current will be pointing upwards right, it will be pulling current out of this node, and that will pull current of the capacitor, and the output voltage will reduce. So, this is consistent.

And basically the small signal picture, we want to have for the voltage buffer is just this, the drain can be connected to ground, because we are not using it at all. The input is applied to the gate of the transistor. And at the output, you can imagine a parasitic capacitor, so that you can visualize this current going somewhere if v_i is different from v_o. And the output v_o is taken from the source of the transistor. So, this is all circuit. Now, clearly in this you can see that in steady state, this current here through this capacitor has to be zero, I mean really nothing is connected to it as far as dc is concern. So, this current has to be zero. And how will this current be zero, this current can be zero only if v_{gs} is zero; and if v_{gs} has to be zero, $v_o = v_i$, the output and input voltages have to exactly equal to each other.

You are familiar with this type of arguments. First imagining that v_o is different from v_i, and then figuring out what happens. We did this while biasing the transistor at a constant current and we are using the same thing again. And now you can see that there is only one possibility here, v_{gs} has to be exactly equal to zero. I have now intuitively shown how this particular topology achieves $v_o = v_i$. We will analyze this in the forthcoming lessons, and see exactly how it behaves. So, at least, by now we should be convinced that $v_o = v_i$, because $v_o = v_i$, this has a gain k equals 1. And you can see whether it has the desirable qualities of voltage controlled voltage source, that is the input resistance is infinity and output resistance is zero and so on. At least one part of it, the input resistance, it is very easy to see. The input is connected to this. I have not shown the complete source it is connected to the gate. The gate current is zero, so the input does not draw any current at all. So, at least it must be clear from this picture that the input resistance is infinite so that part is satisfied. So, the other part, the output resistance will analyze in the forthcoming lessons.