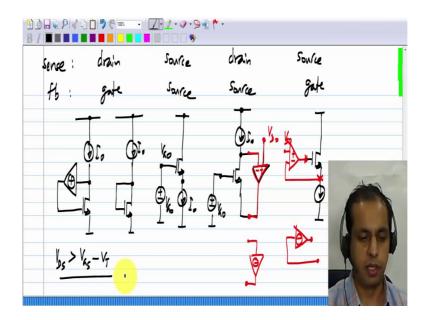
Analog Circuits Prof. Nagendra Krishnapura Department of Electrical Engineering Indian Institute of Technology, Madras

Module - 04 Lecture - 10

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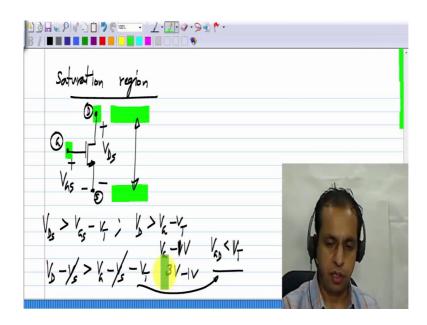
We have discussed for varieties of biasing transistor at a given current I_0 , and central to all these circuits is negative feedback. So, far our discussion has focused on the sense of negative feedback, when you use these things in an amplifier, you also want the transistor to be in saturation region; that means, that you have to get the sense of feedback correct as well as you have to get the bias voltages and so on correct so that the transistor remains in saturation. Now, we will discuss few of these issues. I will show all four types of setting a bias. The very first one was sensing at the drain and feeding back to the gate, the feedback to the gate has to be through a positive incremental gain, and you can do that.

Of course, the variant that we used because positive incremental gain also includes simply connecting it directly; by the way, I keep using the term gain here to describe this circuit positive incremental gain and so on. I do not really mean that it has to provide amplification that is the variation at the output does not have to be more than the input, it can work even if it is less. What I really mean is the sense of variation of output as the input is varied for this block. So, these two circuits are the same where this positive incremental gain is simply

replaced by the wire. And we also looked at sensing at the source and feeding back to the source where the gate is biased at a fixed voltage V_{G0} , so it really means that I have a voltage source V_{G0} or it is derived from a voltage divider and so on. I have I_0 here, then we looked at sensing at the drain and feeding back to the source, where we connect the current source to the drain. The gate is biased at some V_{G0} , and an example was to use an op amp. In general, this part of it that I will show in red, this can be any circuit that has a negative incremental gain.

And lastly we sensed at the source and fed back to the gate, and the circuit looks like this. This is the example that we took and this I call V_{s0} so that means, that it is connected to a voltage source value of V_{s0} or it somehow biased at V_{s0} . And in general, circuitry from there to there, it can be any circuit with a negative incremental gain. So that is the idea. Now, after you do this, there are, of course, many realizations possible for this positive incremental gain or these negative incremental gains and choice of these bias voltages V_{D0} , V_{s0} and so on. After that you have to check separately and ensure that the transistor is in saturation so; that means, that V_{DS} is more than V_{GS} - V_T . So, I will show it for a couple of examples and you can work it out yourself from assignment problems or activity problems and you can even create your own examples.

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So, first of all, saturation region of a MOS transistor is defined by the drain source voltage V_{DS} being greater than V_{GS} - V_T . There are many other ways to put this, sometimes this is

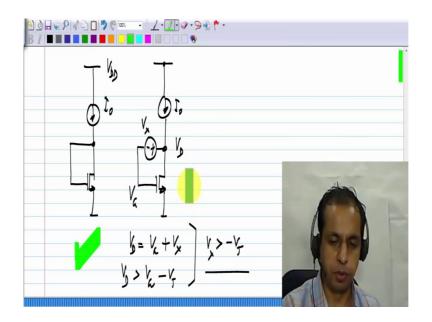
convenient to use when you can calculate V_{DS} and V_{GS} . Now, V_{DS} can also be written as $V_D - V_S$ where V_D and V_S are the drain voltage and the source voltage with respect to some ground. And similarly, V_{GS} can be written as $V_G - V_S$ where V_G and V_S are gate and source voltages with respect to the same ground, - V_T . Clearly you see here that V_S cancels out and the same thing can be equivalently written as V_D being more than $V_G - V_T$.

What does it say? So instead of even computing V_{DS} , you can just compare the drain voltage with the gate voltage. What is this saying, the drain voltage has to be more than gate voltage minus V_T , and V_T , in general, can be negative or positive, although for the most often used variety of transistor it is positive. So, we will continue the discussion assuming that V_T is positive. So, what is this saying, the drain voltage can go below the gate voltage, but not by more than one V_T . So, one way to visualize the transistor going into the triode region is to imagine this separation between the drain and source in terms of voltage of course, the voltage separation between drain and source becoming too small. So, if you have the drain at the same voltage as the source, V_{DS} will be zero and you will be operating at the origin of the I_D, V_{DS} characteristic, it will be in deep triode region.

As this voltage, as this separation increases, it goes towards saturation region; and if this separation exceeds $V_{GS} - V_T$, it will be in saturation region. Another way to think about it is the drain voltage going below the gate voltage that itself is allowed, because V_T is positive, so V_D has to be greater than some voltage that is smaller than the gate voltage. In our example, we have been considering V_T of 1 V, so ($V_G - 1$ V). So, if V_G is 3 V, this means that the drain voltage has to be more than 2 V, it can go below the gate voltage, but not by more than one threshold voltage. So that is another way to think about it. And if you rearrange these things, you can also see that V_{GD} has to be less than V_T that is another way to think about it. I mean it is just the rearrangement of the same relationship, the gate drain voltage has to be smaller than V_T .

All these are restatements of the same thing, but depending on the circuit configuration one of these three relationships is actually easier to use than the others. So, this is just an aside, because I am going to discuss this with respect to the circuits that we already have.

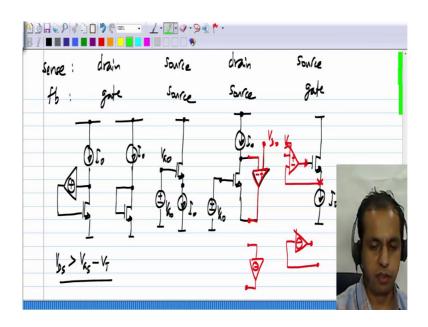
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The very first circuit sensing at the drain and feeding back to the gate, this is what we had. And we know the sense of feedback and the simplest variety was to just connect the drain to the gate, and this we know this will be in saturation region, because the threshold voltage is positive; that means, that V_D will be more than $V_G - V_T$, because in this case, after all, V_D equals V_G . So, this will be in saturation region. Now, another alternative which you would have seen in some activity questions or even discussed it in one of the earlier lessons is to have a voltage source. So, let us I call this V_x then now you see that V_D and V_G are not the same; $V_D = V_G + V_x$; and V_D has to be greater than $V_G - V_T$. So, from these two, you can see that V_x has to be greater than - V_T .

I have shown this with the positive polarity to the right towards the drain. Now, this V_x could be negative, but it cannot be more negative than one threshold voltage. If V_x is - 0.5 V, this will be in saturation region, but if it is - 1.5 V, this will go into triode region.

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So, that is as far as this particular circuit is concerned and this is true in every case because just for biasing for instance, in this case, nothing else is connected, in this case, nothing else is connected to the drain and so on. But when you turn this into some small signal incremental functionality, something will be connected to the drain; so you have to evaluate the saturation region separately that is what I am trying to say. The feedback has to be in the correct sense and the transistor has to be in the saturation for it to behave like a good amplifier.

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Let me consider an example where we sense at the drain and feedback to the source. We have the MOS transistor; to sense at the drain, we connect a current source I_0 . And the drain current I_D is the current through the MOS transistor. We have the gate voltage V_{G0} , and the feedback loop is completed with some block which has a negative incremental gain. I will use an op amp with this polarity; we saw earlier that this maintains negative feedback around the transistor, as well as the op amp and that, is generally the case. And this point is connected to some fixed voltage, let me call that V_{D0} . So, now because of negative feedback around this, the current through the transistor will be I_0 , and how does that happen by having the appropriate value of gate source voltage.

Now, assuming that the transistor is in saturation, the gate source voltage would be the threshold voltage plus square root of two times the drain current divided by the current factor. So, now the voltage at the source would be V_{G0} minus this voltage, - V_{GS} , which is

$$(\dot{\iota}\dot{\iota}G0-V_T-\sqrt{\frac{2I_0}{\mu_n}C_{ox}(\frac{W}{L})})$$
. Now, the drain voltage here, what is that you can figure $\dot{\iota}$

out the value by realizing that the op amp inputs are virtually shorted, because the op amp is in negative feedback, so these two inputs are at the same voltage, so the drain voltage is V_{D0} . Now, how do you verify whether the transistor is in saturation region? By comparing the drain voltage to the gate voltage or drain source voltage to gate source voltage.

In this case, it is easier to compare drain voltage to the gate voltage, we know that V_{D0} has to be greater than ($V_{G0} - V_T$) for the transistor to be in saturation region. So, What decides whether the transistor is in saturation in this particular circuit are the values of V_{D0} and V_{G0} . And you have to choose them appropriately so that the transistor is maintained in saturation. And of course, there are circuits where you may want the transistor to be in triode region, again you have to choose the values of these things appropriately so that the transistor remains in triode region.

So, in summary, when you bias a transistor at a constant current, you are establishing a negative feedback loop, we know how to make the loop to have negative feedback that is eventually the circuit should settle to a point where the drain current is exactly equal to the desired current. If the drain current is more than desired current, somehow the gate source

voltage must reduce; and if the drain current is less than the desired current, the gate source voltage must increase. So, negative feedback ensures that, but of course, negative feedback only tells you in which direction to vary things. The absolute values of voltages are also important to maintain the transistor in saturation region. And you have to pick that appropriately. The negative feedback loop can be completed by a variety of means; in each case, you have to separately check and make sure that the transistor is in saturation.