Analog Circuits
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Module - 04
Lecture – 09

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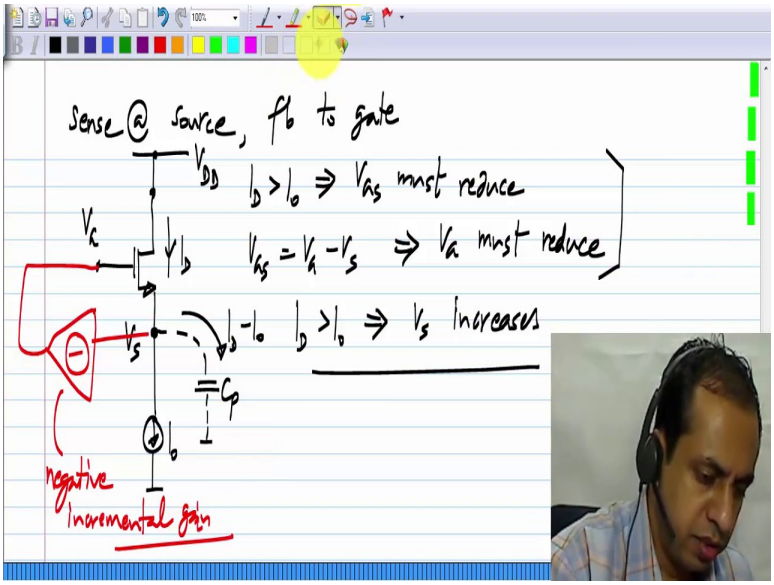

We have yet another alternative, which is to sense at the source and feedback to the gate because the drain is not in this picture; we are sensing at the source and feeding back to the gate I will connect the drain to the supply voltage. It is some voltages, it is connected somewhere. As far as the biasing circuit is concerned, it is not relevant where the drain is connected to; of course in an amplifier, we would like it to be connected such that it remains in saturation region. Now, to sense at the source, I connect the current source I_0 to the source terminal; and we have the actual drain current I_D in the MOS transistor. Now, we are feeding back to the gate.

Earlier, in our very first case, we were feeding back to the gate and we connected the source terminal to ground. But of course, now we are sensing the current difference at the source terminal, so we cannot connect the source terminal to ground. So, the source terminal is connected to the current source, and we have to feedback to the gate. Now the source terminal is not exactly fixed but still, we can go through our chain of reasoning. If I_D is too large, that is, that

larger than I_0 what must happen? V_{GS} must reduce. So V_{GS} must reduce. We do not know what the source voltage is but because V_{GS} equals V_G - V_s. If we are trying to control it with V_G along then this says that V_G also must reduce. And this is the feedback action that we want, that is, if I_D is larger than I_0 then we must reduce V_G So that I_D tends to reduce.

Now, let us see what actually happens at the source terminal; I_D - I_0 flows into the capacitor. And if I_D is higher than I_0, what happens is that the source voltage V_s actually increases. So, what is happening to the source voltage is the measure of whether I_D is greater than I_0 or less than I_0. If I_D is greater than I_0, V_s increases. And we want to reduce V_G so that means that like in the previous case, there must be a negative incremental gain between V_s and V_G that is if V_s increases, V_G must reduce and vice versa. So, we can connect some block that takes V_s as input, and puts out V_G and it must have a negative incremental gain meaning its output reduces as the input increases. So that is the meaning of negative incremental gain.

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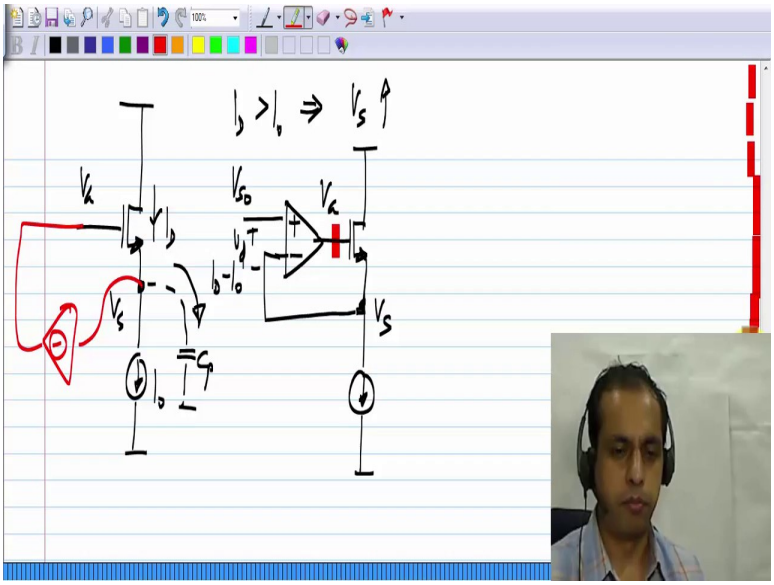

Now, one thing you observe here is that from our earlier discussion you know that this is V_G and I connect I_0 to the source terminal, and there is actual drain current I_D. And if I_D is greater than I_0, I_D - I_0 flows in this direction into the capacitor and raises the source voltage. Now the current I_D is also dependent on the source voltage, so as source voltage increases, I_D tends to reduce. So, there is already feedback just by this connection. And in fact, if this voltage - the gate voltage

was fixed this is our older circuit; this is sensing at the source and feeding back to the source. So, when you connect a current source to the source terminal, there is already feedback to the source. This you cannot remove because source belongs to the controlling part of the MOSFET as well as the control part of the MOSFET.

Now, when you connect this additional circuitry here, there is also feedback to the gate. So, really this circuit, although I called it sensing at the source and feeding back to the gate, we are sensing at the source that is correct but the feedback is both to the source and the gate and both are in the appropriate direction, because if I_D is more than I_0 then V_s increases and through this negative incremental gain, V_G reduces. So, V_{GS} definitely reduces. But this is still a different case from the earlier case we discussed where the gate voltage was fixed, because now you are feeding back to both the gate and the source, and typically the feedback to the gate is much stronger, so it is useful to treat this as a special case. So, we have now discussed all four cases, sensing at either drain or source and feeding back to either gate or source.

Again this circuit is slightly more complicated than the first two types of feedback biasing that we discussed. So, just for a common source amplifier, you would probably not use this, but there are many other circuits in which such an arrangement appears. And I will quickly show you one possibility again using an ideal op amp. I had to sense V_s and feed it back to the gate, and I_Do it through an op amp; and the other terminal of the op amp, I call V_{s0}. Now, we know that we want a negative incremental gain between this V_s and V_G, so it has to be of this sort. The signs of the op amp must be like this. And this is the differential voltage with op amp.

Now, if you look at rest of the circuit from this V_G to V_s, you will find that these are the correct signs for the op amp to ensure negative feedback around the op amp itself because the op amp gives you this virtual short property only when it is in negative feedback. As far as we are concerned we can say that the op amp must be in negative feedback that is all. There are some useful circuits where the op amp may be in positive feedback, but as far as we are concerned in all our op amp circuits, the op amp will be in negative feedback.

So, this concludes the four types of bias circuits that is sensing at the drain, feeding back to the gate; sensing at the source, feeding back to the source; sensing at the drain, feeding back to the source; and sensing at the source, and feeding back to the gate. So, as long as you understand the

basic principle, it does not matter in what exact manner these things happen meaning we may connect the drain directly to the gate, or we may have some other circuitry in between and so on. You should be able to analyze all of them because now you know exactly why these circuits establish the correct operating point current in the transistor.