Analog Circuits
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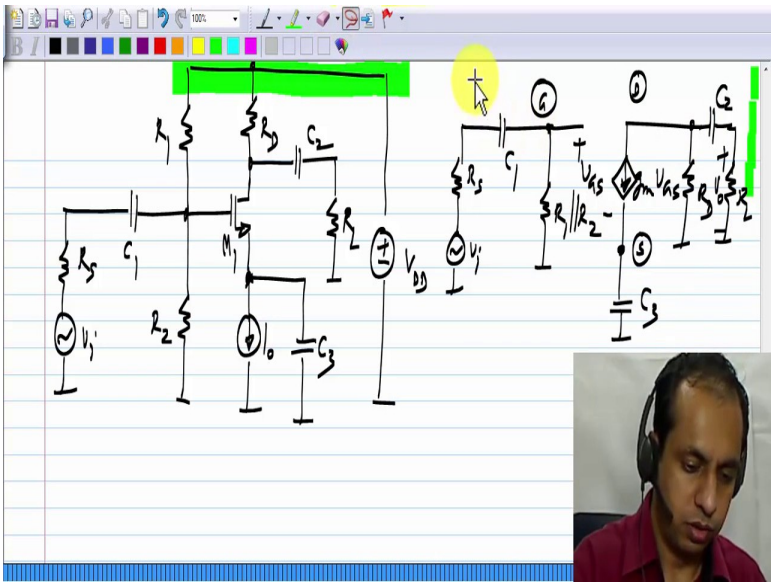
Module - 04
Lecture – 07

(RefeR slide Time: 00:00)



So, this is the small signal incremental picture and we have to make sure that C_1, C_2 and C_3 are shorts at the signal frequencies. How do we do it? As before we do it one by one; we do not try to evaluate the transfer function between V_i and V_o including all three capacitors and it is not worthwhile doing because what we want to constraint, we are going to be making the capacitors much larger than this constraint. So, now while evaluating the constraints for C_1, we assume that C_2 and C_3 are short circuits and so on.

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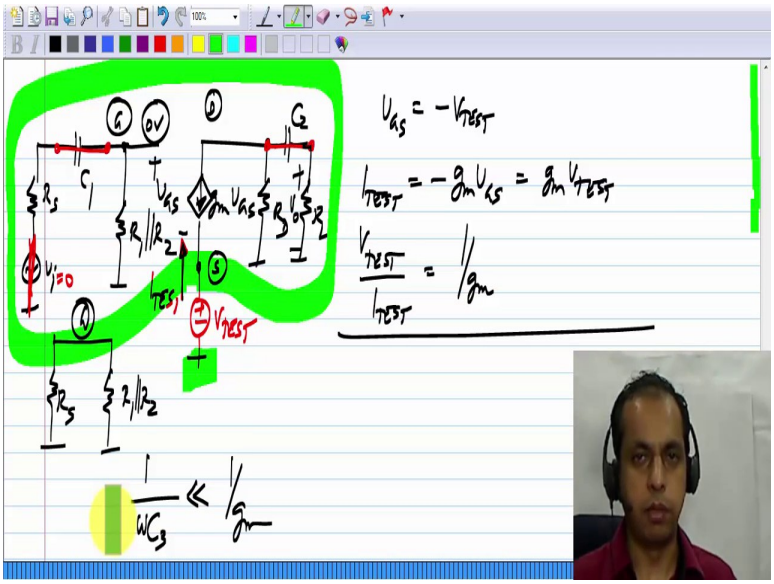

And our usual method is to find the resistance that appears across the capacitor and make sure that the capacitive reactance is much smaller than that much smaller than that resistance. And we deactivate the input, we said V_i equal to zero. Now, C_1 is very easy, you have this loop, V_i is zero, so that means this is the short circuit. And what appears across C_1 is $R_s + R_1 \parallel R_2$. So we want the reactance of the capacitor C_1 to be much smaller than the resistance across it, which is $R_s + R_1 \parallel R_2$. And again when we deactivate the input source, this current source drops out, it turns out you can work it out and see, it will drop out, it will become an open circuit, because it has zero value. And if we look in this loop, this part is open circuited, we have C_2 and $R_D + R_L$ across it. So, the reactance of C_2, $1/\omega C_2$ must be much smaller than $R_D + R_L$. I have repeated this many times by now. This condition ensures that the output voltage here V_o would be same as replacing C_2 by a short circuit.

Now as before we can have another condition, which is relevant when R_D is very large, we want the drain source voltage the voltage at the drain here to be nearly the same as the output voltage. And in that case, the constraint is stronger and $1/\omega C_2$ has to be much smaller than R_L. And again these are things that you are already seen before, so I am not going to spend much time on this. Now we still have this capacitor C_3 that is left, let see how to calculate the constraint for that. Let us assume that C_2 and C_1 are actually short that, means that they have been chosen to be

sufficiently large so that they are shorts at the signal frequency. But of course, while carrying out this exercise V_i set to zero, so this is also a short.

Now, where is C_3 connected, C_3 is connected between this point and ground and the reactance of C_3 must be much smaller than the resistance that appears, because of the rest of the circuit between this point and ground. So what I have to do is to find the resistance between this point and ground and that is quite easy. How do I do that? I apply a test voltage V_{TEST}, evaluate the current that is flowing there, which I will call I_{TEST}, and V_{TEST} by I_{TEST} gives me the resistance. Now, how much is that first of all, the gate voltage is zero, because this is connected to zero, this is a short and you just have R_s and $R_1 \parallel R_2$. So if you look at this part of this circuit, we have R_s and $R_1 \parallel R_2$, when the gate voltage is zero. So this is that zero volt; there is no current flowing anywhere.

So now V_{GS} in this is $V_G - V_S$, and V_S is nothing but V_{TEST} – the source voltage is V_{TEST}. So V_{GS} equals $-V_{TEST}$, it is $0 - V_{TEST}$. And what is the current I_{TEST}? That is equal to the negative of this current, this g_m times V_{GS} is flowing downwards, the I_{TEST} is opposite to that. So I_{TEST} is $- g_m V_{GS}$, and V_{GS} itself is $-V_{TEST}$, so we get $g_m V_{TEST}$. And V_{TEST} by I_{TEST} is $1/ g_m$. So, the resistance between these two points where the capacitor was connected is $1/ g_m$. And the reactance of the capacitor C_3 has to be much smaller than $1/ g_m$. Remember, when we had this drain feedback structure when the gate is connected to the drain, the small signal resistance of the equivalent two terminals element is $1/ g_m$. Here, if we have a similar result, if you look into the source of a transistor, you will end up getting $1/ g_m$. So, please analyze this by yourself and convince yourself that the resistance that appears between these two terminals, because of this circuit is $1/ g_m$. And that gives you the constraint for the capacitor C_3. So, this way we can find all the capacitor values and design our common source amplifier properly.