Analog Circuits
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Module - 04
Lecture – 06

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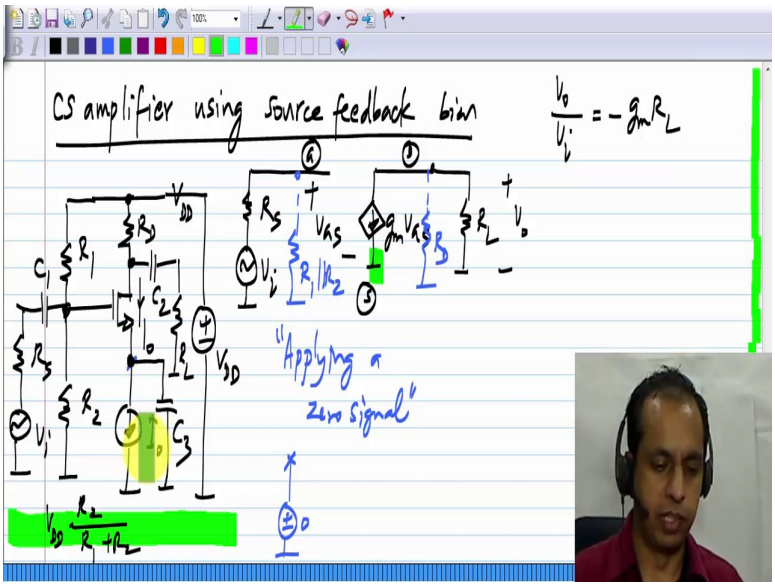

We discussed another method of establishing a constant bias current in a transistor that is source feedback biasing. We connect a current source to the source terminal of the MOS transistor. Now, what we will try to do is to realize a common source amplifier, which incorporates this type of biasing. So, our bias picture looks like this. The gate is biased at a constant voltage V_{G0}, and a current source I_0 is connected to the source, and the drain is connected to V_{DD} because in the biasing picture the drain plays no role. The common source amplifier looks like this. The signal is applied between the gate and source, and the output is taken between the drain and source. This is the drain, this is the source and this is the gate.

And let me change the notation for the input, let me call this V_i for the input signal and the output appears between here. And this amplifier provides the gain of - g_mR_L. From earlier experience, we know that we could have some extra components, it could be for instance from here to ground, and it could be from here to ground or even elsewhere between the gate and drain for establishing bias. So, those things may be there that we will see. Now, the question is how do we bias the transistor like this and make it look like this for the signal picture. So that is what we have to do. So, we will take it step by step. Here, we have used a

voltage source here, and a voltage source there. We do not want to do that we want to use a single supply.

So, how do we do that? First part is very easy. To derive the gate voltage from this main supply voltage V_{DD} all I have to do is to use a resistive divider; R_1, R_2. And this is the supply voltage V_{DD}, and the gate voltage will be $V_{DD}\frac{R_2}{R_1+R_2}$ and we can set this to anything we want by suitably choosing the values of R_1 and R_2. Then the signal source must be applied to the gate of the transistor. How do we do that? I would not spend much time on this, we have done this many times now. This part establishes the bias to add the signal from this, what we have to do is V_i, R_s and connect a coupling capacitor C_1.

Now, we have to be able to connect the load, and the drain cannot be connected to the supply voltage directly. If we do, we know that we can connect the load to the drain by ac coupling so that the dc value is blocked, and only the signal appears here. But, if this is connected directly to V_{DD}, the drain is connected directly to V_{DD}, V_{DD} is nothing, but ground in the incremental picture. So that means, that this will be connected directly to ground. So, if it is connected to ground, then the signal voltage being here will be zero, so that cannot be permitted obviously. We want some signal to come out of the amplifier. So, the drain has to be connected to V_{DD} through a bias resistor R_D. It has to get connected somewhere, so that this I_0 has some path to flow and it has go to V_{DD}, but it cannot be connected directly to V_{DD}, because in that case that is like shorting the output of the amplifier to ground.

Basically, if we connected directly to V_{DD}, we will have a short circuit here right from the drain to ground. So, then clearly the gain will be zero, it will be g_m times the zero resistance. So, what we need to do is connect it through this resistance R_D and then if we do both of these what happens is that we will have a resistance R_D from drain to ground in the small signal incremental picture, and $R_1 \parallel R_2$ from gate to ground in the small signal incremental picture. And this is the same as, in a couple of cases we have seen earlier, the common source amplifier with constant voltage bias at exactly these things.

Now, you can see that one thing is left out, there is one difference between this and that. The source of the MOS transistor must be connected to ground in the small signal picture. That is why it is a common source amplifier so that the input is applied between gate and source,

output is taken between drain and source. If you look at the source terminal of the MOS transistor in our actual circuit, it is certainly not connected to ground. If we draw the incremental picture from this picture on the left side, I_0 will become an open circuit and the source is not connected anywhere. So, if you do that you can analyze it and see, and the gain will again be zero. So, this has to get connected to ground for signals. And as usual, as always we have made the assumption that signal frequency has a certain minimum, which is not zero that is why we are able to couple the input through a capacitor, take the output through a capacitor and so on.

And we can use the similar idea to connect the source to ground for signals. When we say we have to connect the source to ground, essentially you can think of it as applying zero signal to the source of the transistor. So let us say I have source that is zero and the source of the MOS transistor has to get connected to this. Essentially, it should get shorted to ground for signal frequency, so; that means, that we have to couple it to the ground or the zero voltage source through a capacitor. So that is what we will do. We will connect it to ground through a capacitor, let me call it C_3.

Now, as before, if the capacitor is sufficiently large, what happens is that it will act like a short circuit, and it is as though the source is connected to ground. We have to evaluate the criterion of C_3 to behave like a short circuit that we will do later. So, what we did was the following. I went through this pretty quickly because by now you are familiar with the principles of ac coupling and the input and the output. The only thing special here was with this biasing scheme, the source terminal of the MOS transistor is not connected to ground. In the drain feedback case, the way we started off it was connected to ground, but here it is not. So, we have to connect it to ground for signal frequency through a capacitor C_3. So, this circuit now is yet another topology of a common source amplifier, it uses source feedback biasing.

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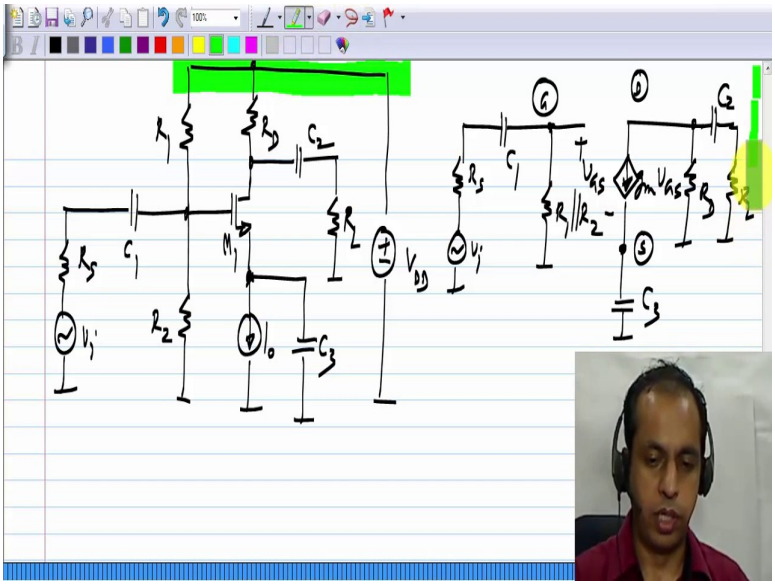

I will redraw the circuit here. I have the signal source, its ac coupled to the gate of the transistor. And the gate is biased using a resistive divider, which is powered from the supply voltage V_{DD}. And the source is biased by connecting a current source to it. A path for the drain current is created to V_{DD}, through a resistor R_D. Finally, we have to evaluate the drain source voltage of this transistor M_1 and make sure that it is indeed in saturation region. And the load will be coupled through a second capacitor C_2, finally, the source of the transistor is shorted to ground using a capacitor C_3.

Now, if I draw the small signal incremental picture of this; we will have the input source V_i, R_s and it is connected through capacitor C_1 to the gate of the MOS transistor. And from the gate of the MOS transistor, we have these two resistors R_1 and R_2, and in the incremental picture this point here the supply voltage is also ground, because this supply voltage does not have any increments at all. So, we will have R_1 and R_2 from this point to ground; in other words, $R_1 \parallel R_2$. Then, we have our controlled source of the MOS transistor, this is V_{GS} and that $g_m V_{GS}$. This is the drain, this is the source terminal and from the source terminal to ground, we have the capacitor C_3. This current source is an open circuit because it is a fixed current source. And from the drain to ground, we have R_D and a capacitor C_2, and the load resistor R_L. So, this is the small signal incremental picture and we have to make sure that C_1, C_2 and C_3 are shorts at the signal frequencies.