Analog Circuits
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Module - 04
Lecture – 02

We will now see how to realize the common source amplifier using current mirror biasing. Earlier, we have used a drain feedback around the transistor, to set the transistors drain current to be equal to some given current I_0, and use that transistor as a common source amplifier. Now, with a current mirror biasing, we can have feedback around just one transistor, but replicate its bias around many other transistors, and realize common source amplifiers with all of them. Of course, the condition is that all these transistors must be matched and must be on the same IC, same dye so that they are all at the same temperature and so on.

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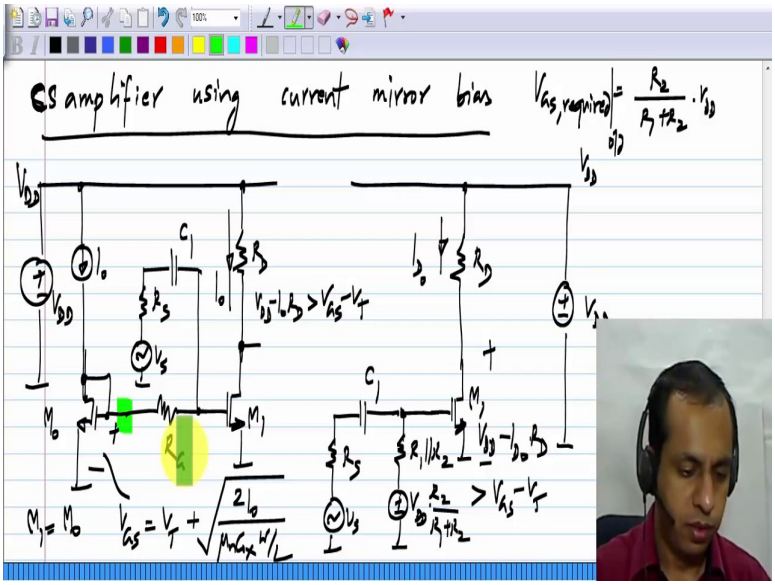

So, we will realize the common source amplifier using current mirror bias. Now, what is the current mirror bias? This upper line is assumed to be the supply voltage V_{DD}. I have not shown it always our explicitly point it to it when I felt it is not necessary, but now I will show that. Here, we have drain feedback around this transistor M_0. And this gets biased with a V_{GS},

which is $V_T + \sqrt{2I_0/\mu_n C_{ox}(\frac{W}{L})}$, and as I have pointed out earlier, this itself V_{GS} being this gives you correction for any deviation in V_T or current factor and so on. Now, I do not want to realize the common source amplifier using M_0, we have already seen that. We can have a resistor between drain and source, and we can ac couple to the input and output and so on, so that is what I do not want to do.

We have another transistor M_1, and M_1 and M_2 are matched. I want M_1 to have the same operating point current I_0, and I want to realize a common source amplifier using M_1. How do we do this? Now I can just explain to the circuit, but it is useful to recall how it did for the constant voltage biasing. So, what did we do then? We had our supply voltage V_{DD}, which of course, means that there is a voltage source of V_{DD} between that line and ground. And we had our transistor M_1, what we did was we knew what V_{GS} we wanted, and we use the voltage divider to get that. V_{GS} required in that case, I will call it old to recall that this is the old constant voltage biasing technique, is $\frac{R_2}{R_1+R_2}V_{DD}$. And we choose R_1 and R_2 accordingly and we had our signal source V_s, R_s.

Now, we know that between this terminal and ground, this voltage divider is equivalent to a resistor $R_1 \parallel R_2$ in series with the Thevenin source, which is $\frac{R_2}{R_1+R_2}V_{DD}$. So, how did we have this value of bias and this value of signal? We connected this value of bias through a resistor. Now, we did not use an explicit resistor, because this resistor is already in place. So, the bias voltage is connected to the gate through a resistor, and this signal voltage is connected to the gate through a capacitor. Now, we can do exactly the same thing here. The bias voltage is available from here. The V_{GS} required is this one, it is not this some fixed voltage, but it is dependent on the transistor characteristics and the current that we want to have. And we have our signal source. Because of lack of space, I will show it up here, so I have V_s, R_s.

What I want to do is to add this bias to that signal. So, what should I do? I connect the bias through a resistor, I call it R_G. And I connect the signal through a capacitor C_1. As before we

assumed that the signal frequency has some minimum value which is not zero; so if it is zero, you could not do that, because in the capacitor will block dc, but for a lot of applications this is good enough. We can assume that this signal has a certain minimum frequency. In that case, we can choose C_1 to be finite, but large enough. So, now I did this also to show you the similarities between different biasing techniques. In principle, you have some way of getting a voltage here, you add that voltage to the signal. In this case, you have some other way of obtaining the dc bias voltage, and you add that to the signal.

Now, this establishes V_{GS}, this establishes V_{GS} here. We also have to make sure that V_{DS} is more than V_{GS} $-¿$ V_T , for M_1 to be in saturation. So, how did we do that with the common source amplifier? We connected a drain bias resistor R_D, and the current through this was I_{D0}, whatever the operating point drain current of M_1 is. So, the voltage across M_1 is $V_{DD} - I_{D0} R_D$. We have to make sure that this is more than V_{GS} $-¿$ V_T . Now, we can use exactly the same technique here. We can bias it through a drain resistor R_D, by the way, this V_{DD} of course, also means that there is a voltage source of V_{DD} between there and ground. Now, if this is in saturation, the bias current flowing through this will be equal to I_0. This is ignoring λ, slight dependence of the drain current on the drain source voltage.

So, the drain source voltage would be V_{DD} minus $I_0 R_D$. And our assumption that the transistor M_1 is in saturation will be correct if this is more than V_{GS} $-¿$ V_T , which we can calculate and ensure. So, this completes the bias, the transistor is now biased with the voltage that is derived from constant current biasing, so the difference between this one and this one is that V_{GS} here is the constant; so if V_T changes, if V_T increases, the trans conductance here of M_1 will drop. Whereas here these two are matched, so if the threshold voltage increases, this voltage itself will increase to compensate for that. So, there is no change to the g m of this transistor that is why we choose this kind of biasing in the first place, it is better. It keeps the gain more constant.

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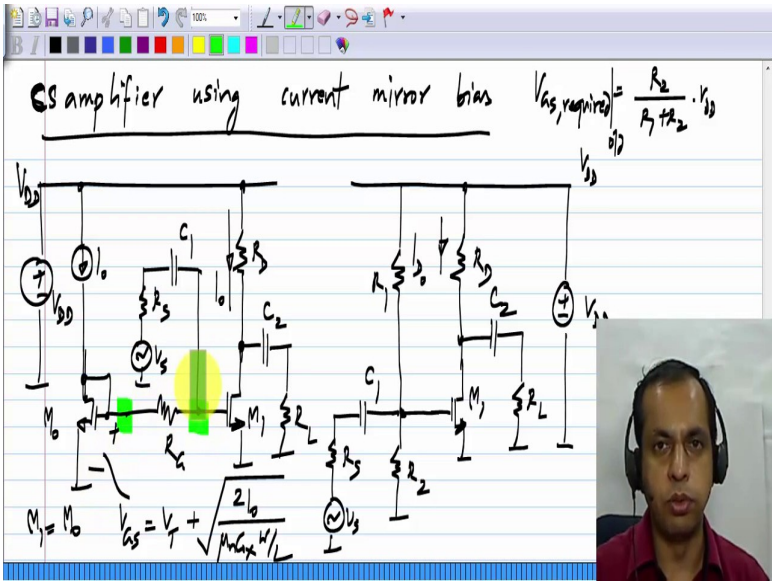

Now, we have to connect the load, and that is very easy. We ac coupled the load to the drain of the transistor, more precisely the load is connected between drain and source, but of course, this is just a representation of the following stage, it may not be a physical resistor. So, we show one terminal as being grounded. Through this capacitor C_2, we couple the load, we ac coupled the load, and as before we can calculate the value of C_2. So, this is what we did with the common source amplifier and that is what we do now. And of course, the original common source amplifier, the gate bias was derived using a voltage divider. I have shown some representation of that. Now, you can see the similarities between these two. The only difference is that this voltage is not constant with respect to transistor parameters. If the threshold voltage increases or the current factor drops, the bias voltage itself increases to compensate for it to some extent.

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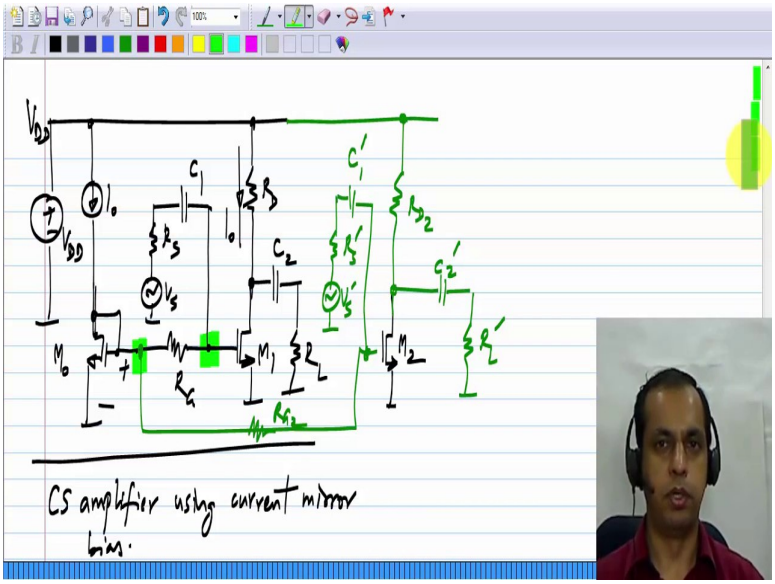

So, this circuit is the common source amplifier using current mirror bias. This R_G, it plays somewhat similar role as before. Essentially this R_G putting it here makes sure that the dc voltage here and there are the same. But this C_1 is expected to be very large, so this point will get shorted to that for signal frequencies. And you have to choose R_G very large so that there is no division of voltage between V_s and the gate. So, I hope this part is clear.

Now, what you can do is for instance, you have another transistor, you want to build a bunch of amplifiers, let say you had M_2, and you wanted the same operating point and so on. You could use the same bias voltage to bias this through a resistor R_G of course, I will call it R_{G2}. The assumption here is that R_G, R_{G2} are all very large, then there will be no interaction between this amplifier and that one. We would not analyze that in detail, but if R_G is very large, it is like having separate amplifiers, so although they are connected to the same node. And whatever signal we want to connect to M_2, we connect it through another one, another coupling capacitor, and we can realize yet another common source amplifier using M_2. So that is another common source amplifier. And you can bias a whole bunch of common source amplifiers with this constant current derived biasing using a current mirror. So that is the advantages of this. I hope that logic of deriving this circuit is very clear otherwise please go through it step by step and make sure that you understand every one of them.