Analog Circuits
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Module - 03
Lecture – 13

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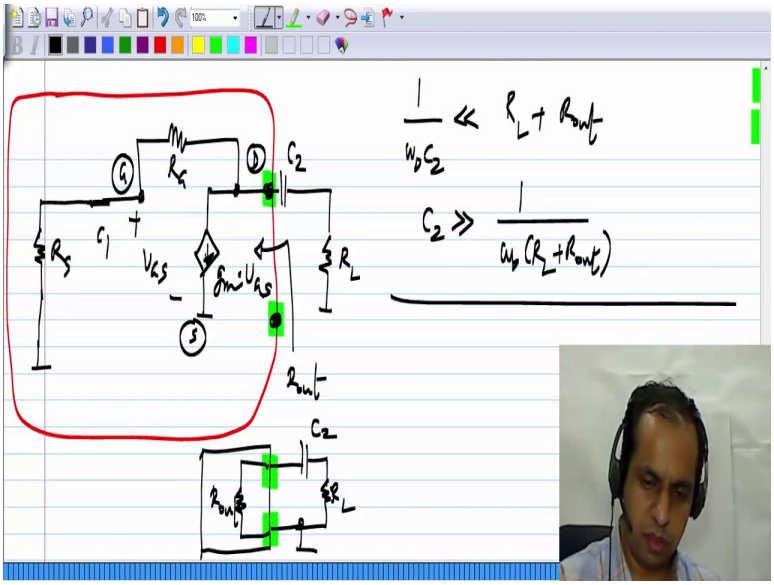
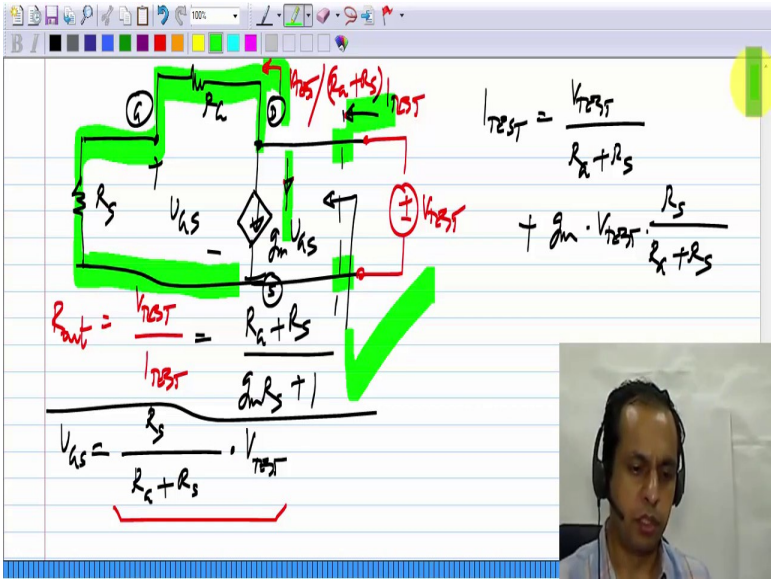


Let us now come to the capacitor C_2; and while computing the constraint for capacitor C_2, the independent source, of course, is set to zero, so it becomes a short circuit. It is a voltage source, which is zero. And the capacitor C_1, we assume has been chosen properly so that is also a short circuit. So now let me draw the box around this circuit. What is the resistance that appears across C_2? You can see that the connection looks something like this. We have this circuit and its output terminals; C_2 is connected here, and R_L is there, and this is the ground. So, between these two terminals between here and there, which are these looking in, you will see a resistance, because it is a linear circuit, you have to see something that will be a resistance and that resistance is nothing but R_{out}, the output resistance of this circuit.

So, all you have to do is to compute the output resistance of this circuit, and make sure that C_2, its reactance is much smaller than the total resistance that is $1/\omega_0 C_2$ is much smaller than the

total resistance which is R_L + R_{out} or C_2 must be much greater than $1/\omega_0(R_L+R_{out})$ (Refer Slide Time: 01:45)



So, what is the value of R_{out}? Again very easy to compute, we have R_s here and R_G between the gate and the drain of the MOS transistor; the control source g_mV_{GS}.This is V_{GS}, this is the source terminal, and we are trying to find the resistance between the drain node and ground. And what do we do? as usual, we can apply a voltage source V_{TEST}, and find the current I_{TEST}, and take the ratio V_{TEST}/I_{TEST}. So again there are many ways to do this. I suggest that you try it by yourself, just as an exercise in circuit analysis. Now, you can, of course, write the usual Kirchhoff's law and find it. What I will do is slightly different from that. I will notice that basically, this voltage source appears across this resistive divider. By the way, if you are getting confused simply write the Kirchhoff's current law at this node, and at this node, and you will find the result.

So, I will do it slightly differently; this V_{TEST} is applied across this resistive divider, and no current is flowing from here, the gate terminal. So this V_{GS} here is nothing but resistive divider ratio times V_{TEST}; $V_{GS}=\frac{R_s}{R_G+R_s}V_{TEST}$. And the current that is flowing up in this branch is nothing

but $V_{TEST} \text{¿} (\text{¿¿} R_G + R_s)$. The current flowing here is $g_m V_{GS}$, which is g_m times this whole thing. So, the total current I_{TEST}, this equals that one plus that one. So, we find that

$$I_{TEST} = \frac{V_{TEST}}{R_G + R_s} + g_m V_{TEST} \frac{R_s}{\text{¿}\ R_G + R_s}$$

And by solving for this ratio, we find that the output resistance is nothing but $(\text{¿¿} R_G + R_s) / (g_m R_s + 1)$, so that is how it is.

And also when you carry out these calculations, it always good to have some sort of sanity checks, some checks where by evaluating some extreme cases, you can see whether the answer make sense or not. And in this case, I can think of one such thing let us say g_m is zero, that is there is no transistor at all; we have only the resistors. Then what should happen? This current source disappears and all you see between these two terminals is the series combination of R_G and R_s. Now in this expression, if you set g_m to zero, the answer is $R_G + R_s$, so it does satisfy the sanity check. And these things are very important; first of all for simply checking that the result that you got after a lot of algebra is correct, and also to get some intuition about the circuit.

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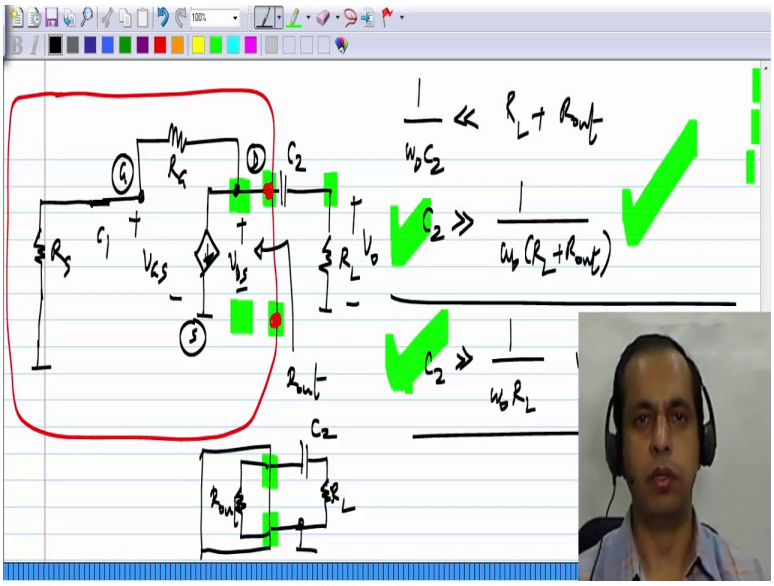

So, once you calculate the output resistance, all you have to do is calculate the constraint on C_2 using this, and C_2 to be much larger than that one. So, that completes our treatment of the common source amplifier using drain feedback. And it works as a common amplifier provided R_G is sufficiently large, we have calculated what that is; and also we have calculated the constraints for the ac coupling capacitors. We already discussed the constraints on capacitor C_2, so that it appears as a short circuit and that is this condition.

Now, like we discussed with the original common source amplifier with a fixed gate source bias, this condition ensures that the gain of the amplifier is the same whether the capacitor is there or not, that is the meaning of capacitor being a short. If C_2 satisfies this constraint then you will get a certain small signal gain and it will be very close to what you would have got if C_2 is really a short circuit or it is an infinitely large capacitor. Now, we also discussed another possible constraint for capacitor C_2; many times we want the voltage V_{DS} here to be the same as V_0. Now, if this condition is satisfied under some circumstances, it possible for this signal V_{DS} across the drain source voltage to be substantially more than the output voltage V_0.

So, we will not V_{DS} to be the same as V_0; in that case, as we discussed earlier, this constraint would be C_2 must be much greater than $1/\omega_0 R_L$. So, many times you use this constraint as

well. And as before obviously, if you satisfy that you will automatically satisfy that one. This is the stronger condition.