Analog Circuits
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Module - 03
Lecture – 12

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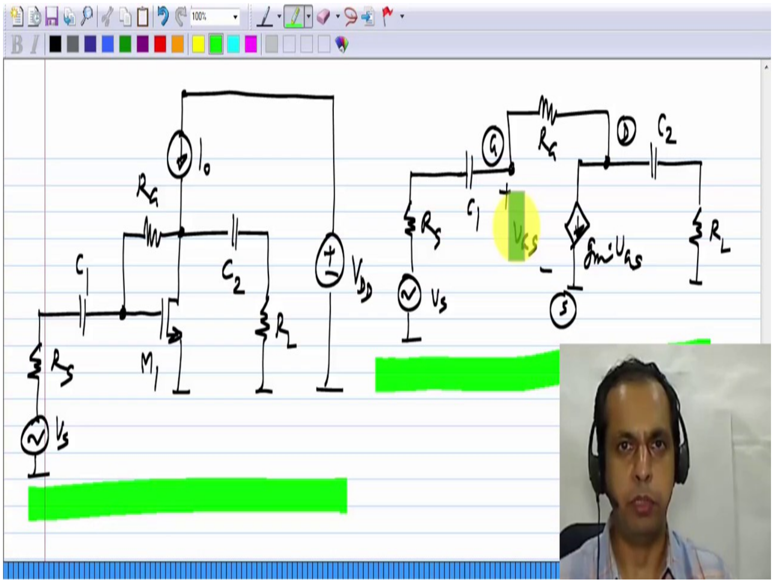

We have analyzed the gain of the common source amplifier using drain feedback biasing and found the constraints for the gate bias resistor R_G. Now, we will do the same thing for the capacitors, coupling capacitors C_1 and C_2. Now, this on the left side is the complete circuit with drain feedback bias and also the input source connected to C_1, the load coupled through C_2. And the small signal equivalent is shown on the right side. All I have done is to open circuit I naught, short circuit V_{DD}, and replace the transistor with its small signal equivalent, and this is what we have. So, let us see what the capacitor values must be so that they do behave like short circuits.

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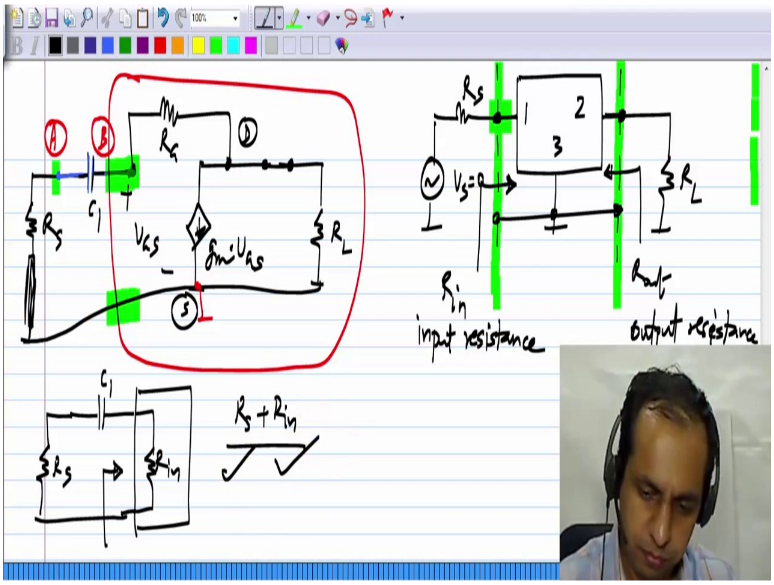

This is the circuit we have, and first, let us focus on C_1. And the input source, of course, is deactivated. The principle we use is as usual to find the resistance that appears across the capacitor and make sure that the capacitor reactance is much smaller than that resistance. And in this process, the independent sources in the circuit are shorted, so the input source V_s is shorted to ground. And also we have two capacitors and we do not want to get into the complication of calculating with both capacitors in place. So, we will make a reasonable assumption that while calculating the value of capacitor C_1, the other one is chosen correctly such that it does behave like a short circuit. So, we will replace C_2 also with a short circuit, while carrying out calculations for C_1.

So, now this is the circuit we have and here are the two terminals of the capacitor. And just for completeness, I will connect it up like that. So, what is the resistance that appears across C_1? Let me draw a box around the rest of the circuit. This is ground, by the way, this point is grounded. So, if you see the C_1 is connected between this terminal A and terminal B; and between B and ground, there is a circuit enclosed within the box. In other words, I have C_1 over here, R_s , and this is connected to something that is actually the circuit. And there will be some looking in resistance. You know that if you have a linear circuit, then the equivalent between any two terminals will be a resistance. So, there will be some resistance inside. And this resistance is nothing but the input resistance of this circuit.

What do I mean by that, when you have a circuit, a two port, some two port one, two and three which is common ground let say. We have V_s and R_s ; and R_L on the other side. In such a situation, the resistance that you see into the input port that is between this terminal and this terminal, this is known as R_{in}. And between this terminal and this terminal, this is R_{out}, that is the output resistance. And the output resistance is computed with V_s being set to zero. So, this is the definition. If you have something that you can identify as the input port, then the resistance looking into that is the input resistance; and something let us identify as the output port, resistance looking into that is the output resistance. It is important to remember that while calculating the input resistance, the load must be in place because this can affect the input resistance. After all, it is to the right side of this circuit.

Similarly, while calculating the output resistance, the source resistance here must be in place. The source itself would be set to zero, but the source resistance would be in place. So, between these two terminals, between this point and that it is nothing, but the input resistance of the circuit. So, this also kind of gives us an experience of calculating input and output resistances of amplifiers. And across C_1, you clearly see that we have R_s + R_{in}. R_s we already know, R_{in} is what we have to calculate.

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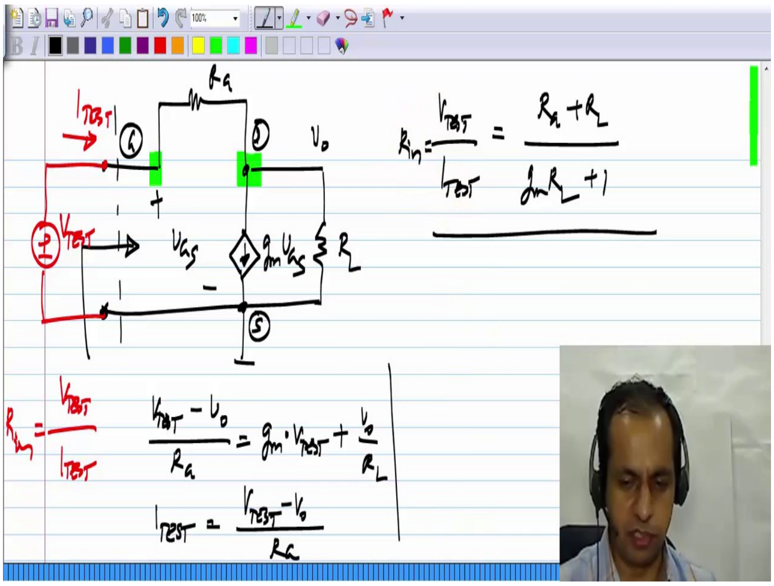

$$R_{in} = \frac{V_{TEST}}{I_{TEST}} = \frac{R_G + R_L}{g_m R_L + 1}$$

$$R_{in} = \frac{V_{TEST}}{I_{TEST}}$$

$$\frac{V_{TEST} - V_o}{R_G} = g_m \cdot V_{TEST} + \frac{V_o}{R_L}$$

$$I_{TEST} = \frac{V_{TEST} - V_o}{R_G}$$

So, let me put down that part of the circuit again. This is the gate, drain, and source, which is grounded; and across this, we have R_L. This is $g_m V_{GS}$, where this voltage is V_{GS}. And we have to calculate the resistance looking into these two terminals, and you know from basic electrical circuits that the way to do it is by either connecting a voltage source and measuring the current that is flowing through it, taking the ratio or applying a current source, finding the voltage that develops and taking the ratio. And in this particular case, I will connect a voltage source V_{TEST} and find the current I_{TEST}. So, all we have to do in that is to write the Kirchhoff's current law here. In fact, I would encourage you to stop the lecture right here, and find this I_{TEST} and the ratio $\overset{V}{\underset{¿}{(¿¿TEST/I_{TEST})}}$ which will be the input resistance. So, please do this by yourself, I will show you the answer, but of course, it will be a better learning experience if you do it by yourself.

So, if I write Kirchhoff's current law equation here, let me call this V_o, the voltage here is V_{TEST}. I have $\overset{V}{\underset{¿}{(¿¿TEST-V_o)/R_G}}$ that is the current being pumped into the output node through R_G. And that current will be equal to the current that is flowing out of here, which is g_mV_{GS}; and you see that V_{GS} is exactly the same as V_{TEST} in this case, so it is $\overset{g}{\underset{¿}{(¿¿mV_{TEST}+V_o)/R_L}}$. And you also see that this current I_{TEST} here is nothing, but the current flowing through R_G, so I_{TEST} equals $\overset{V}{\underset{¿}{(¿¿TEST-V_o)/R_G}}$. And you can eliminate the variable V_o from this equation and find V_{TEST} by I_{TEST}, and hopefully you have tried this by yourself and you got it correctly and the correct answer is $\begin{array}{c} R \\ g \\ (¿¿mR_L+1) \\ (¿¿G+R_L)/¿ \\ ¿ \end{array}$. So, that is it, you would have chosen some value of R_G, and based on that you can find this R_{in}.

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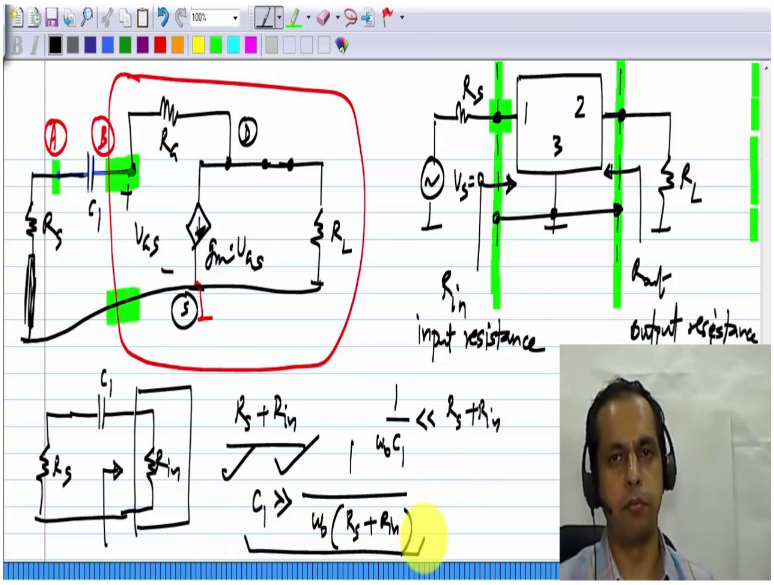

And as far as our capacitor C₁ is concerned, $C_1 \gg 1/\omega_0(R_s + R_{¿})$. If I write it in terms of reactances, the reactance of the capacitor $1/\omega_0 C_1$ must be much less than $R_s + R_{¿}$; and in terms of C₁, it is like this.

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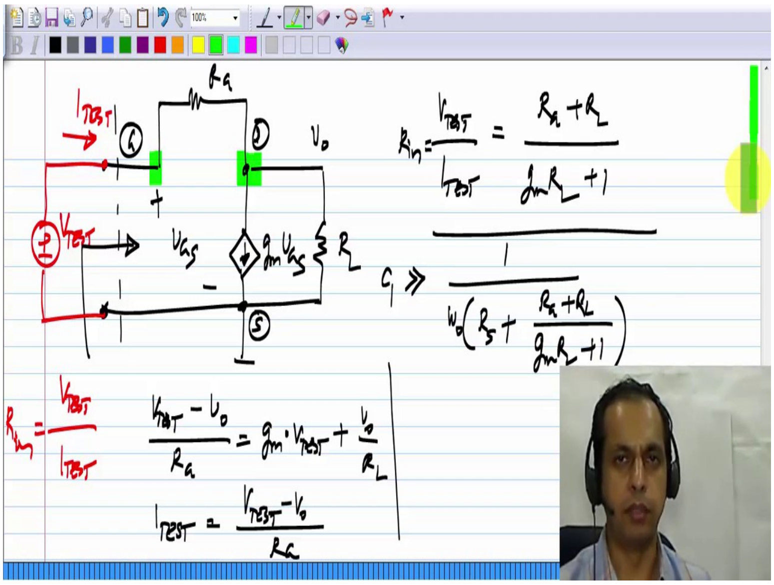

So, C$_1$ has to be much more than $1/\omega_0(R_s+R_{¿})$, where R$_{in}$ is R g $(¿¿mR_L+1)$ $(¿¿G+R_L)/¿$ $¿$. And you can see that although this R$_G$ will be very large, this g$_m$R$_L$ is also a large number because it is the gain. So, the input resistance will be substantially smaller than R$_G$ in this case. So, from this, you can calculate the constraint on C$_1$, and set C$_1$ to be let say ten times or even more compared to the constraint.