Analog Circuits
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Module - 03
Lecture – 10

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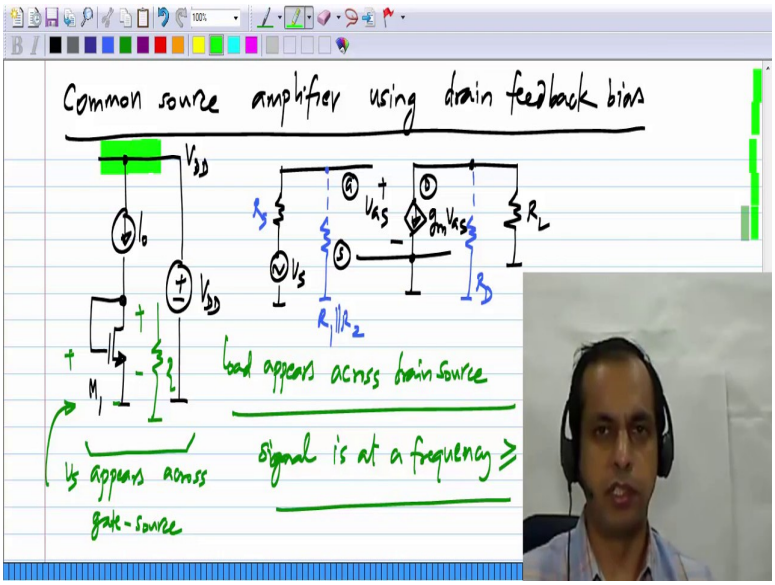

We now know the technique of drain feedback biasing, but our aim is to realize a common source amplifier with smaller gain sensitivity. So, what we have to do is to marry the drain feedback bias with the small signal picture of the common source amplifier and come up with the circuit, which behaves like a common source amplifier in the incremental small signal picture, but its biasing is based on drain feedback. Now, drain feedback bias has this arrangement, the desired drain current I_0 is connected that way and the drain voltage is fed back to the gate, let me call this MOS transistor M_1 and this is V_{DD}, which really means that the supply voltage V_{DD} is connected between this upper rail and ground. So, it is quite common to show sometimes just the line that is marked V_{DD}, it means that there is a battery of value V_{DD} between this point and ground.

Now, what is the common source amplifier? common source amplifier is one where I have a signal source, and I have my transistor, gate, drain and source. And this is the control source inside the transistor $g_m V_{GS}$, where the V_{GS} is the gate source voltage.

The source is grounded and the load is connected between drain and ground, this is the essence of the common source amplifier. Now, of course, we could have extra components, first of all, we could have capacitors, which are useful for adding some value of bias to the signal, assuming that the signal is above a certain frequency. Also, we may have other resistors useful for biasing. If you recall the old circuit, we had R_1 parallel R_2 over here, and then we had the drain bias resistor R_D over there. These may or may not be there that depends on the exact biasing arrangements. But the stuff that I have shown in black that is the common source amplifier.

So, somehow we have to make sure that this signal V_s or most of it appears across this gate source. And then we have a load resistance R_L, and this R_L must appear across drain source. Now, of course, this must happen without disturbing the bias. So, let us try to do this. We already know all the principles we need for this. We know how to add signal to bias. As usual, we will assume that the signal is at a frequency greater than or equal to some ω_0 . So, we do not have dc signals. So, in this case, you can use ac coupling techniques, we can use a capacitor to couple the signal and we know how to calculate the value of the capacitor.

So, given this, we can proceed with trying to turn this into a common source amplifier, so let us do that. As usual, I would encourage you to think through the steps yourself, to find out exactly how to do it, and it is fun, this is how you invent circuits. This circuit we are going to come up with is already well known, but later when you become more experienced, you can come up with new circuits and that is why a chain of logical reasoning just as this one. So, you know certain building blocks and you put together those building blocks to make more complex circuits.

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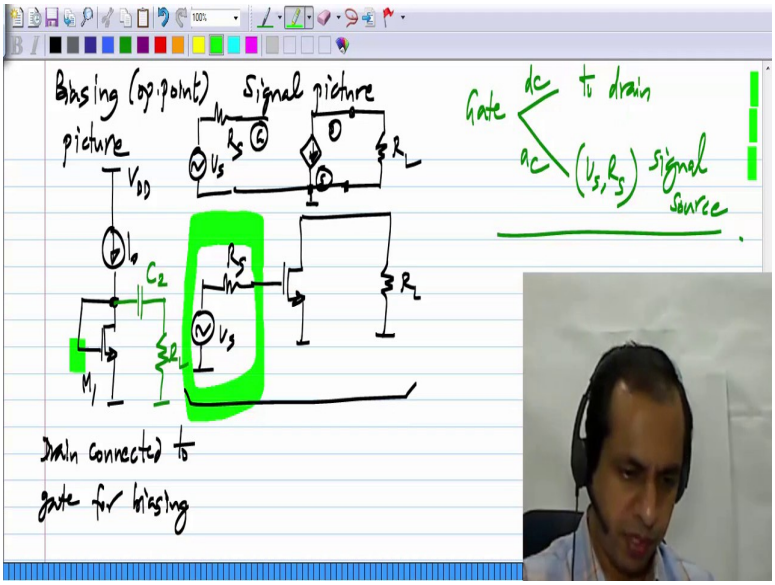

So, we have the biasing picture or setting up of the operating point and in that, I will continue to show it like this. Please understand that there is a battery between this point and ground. This is M_1; so the essential feature here is that drain is connected to the gate for biasing. And the signal picture, I will show a MOS transistor instead of its small signal picture, I could also show that. Let me show both and later depending on convenience, I will show only one or the other. This is the small signal picture, what should happen, this source should be grounded in this small signal picture and the source V_s must appear here. This is the gate, this is the drain, this is the source and R_L must appear over there. And of course, the transistor has to remain in saturation, but that is guaranteed by this biasing arrangements. Because in this case, V_{DS} equals V_{GS} and it is definitely more than V_{GS} minus V_T as long as the threshold voltage V_T is positive.

Or if I draw it with the MOS symbol and have V_s and R_s appearing across the gate source, and R_L appearing over here, this is in the small signal incremental picture. Now, first let us try connecting the load resistor. The load resistor must appear between drain and ground or it must be connected to the drain. So, let me take the load resistor R_L, which could be grounded. This was explained earlier while discussing the original common source amplifier. R_L is the representation of whatever follows it may not be a physical resistor, so one side of it is grounded.

Now, what do I do? It has to get connected to the drain so the first naive attempt is to simply connect it to the drain like that. Now, please think about what problems this could have. One problem that is immediately evident is that we wanted this current I_0 to flow through the drain of the transistor, the drain current has to be equal to I_0. But, in this case, what happens I have a certain value of operating point drain source voltage V_{DS}, and that appears across R_L, so V_{DS} by R_L will flow that way. So, the current in steady state, this drain current will not be equal to I_0, but it will be equal to I_0 minus V_{DS} by R_L. So, this is an unnecessary complication, you do not want this R_L to draw any operating point current, it is totally useless. There is no point in doing that.

So, what do we have to do, we have to connect it differently, we cannot connect it directly. So, somehow only for signals it should appear across this. And that is easy if this signal is above a certain frequency ω_0 . So, this is known as ac coupling and the way we connect R_L to the transistor is exactly the same as our original common source amplifier. We connect it through a capacitor. So, that if the capacitance is very large, then all of the signal voltage V_{DS} will appear across R_L, but the dc here is blocked. So, sometimes this is also known as dc blocking capacitor. The operating point here will be V_{GS}, whatever the V_{GS} is; it is given by ($V_t+\sqrt{2k_nI_0}$), as we have evaluated earlier. The operating point voltage here is zero, and the difference would be dropped across the capacitor. So, let me call this C_2, following my original notation.

Now, what should I do about the gate? The gate voltage must get connected to the drain for dc biasing, but it should get connected to this source combination of V_s and R_s for signal, for ac. For dc, it should go to the drain; and for ac, it must go to V_s R_s, basically the signal source. How do we arrange this? This is again something that we know. We know how to add a certain dc to a certain ac signal source, that is we want a terminal to be connected to terminal A for dc, and terminal B for ac, we know how to do that. This is exactly what we did earlier also.

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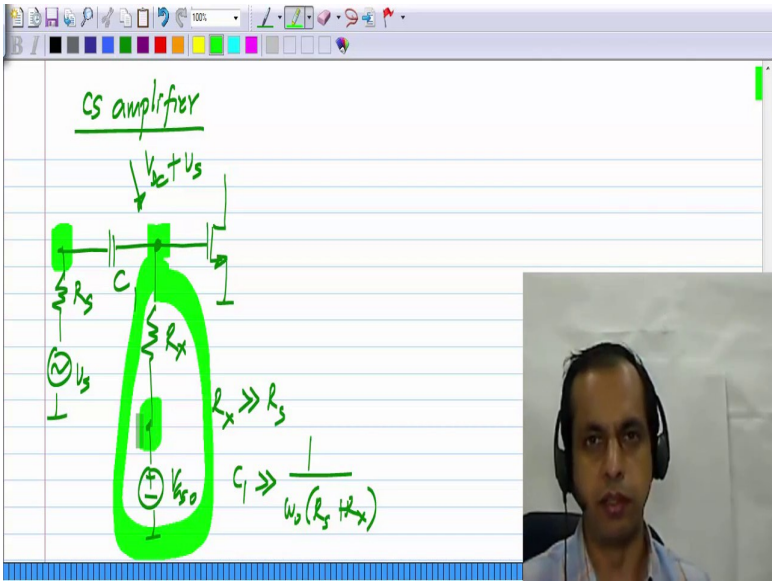

In case of the common source amplifier, if you recall the gate, I would not show the complete picture on the drain side, but the gate we have to get $V_{dc} + V_s$. So, what did we do? We have the signal source V_s and we have the dc source V_{GS0}, whatever the quiescent value, the operating point value of V_{GS} is. How did we do this? So we connected V_{GS0} through some resistor and the signal source through a capacitor. Now, of course, we have to satisfy some more conditions. This R_x has to be much more than R_s so that all of V_s appears here and

$$\omega_0(\text{¿¿s} + R_x) \quad R$$
$$C_1 \gg \frac{1}{\text{¿}}$$

and so on. So, this was the essential idea. Now, of course, in the common source amplifier, we did not have a separate source V_{GS0}, this itself was derived from a voltage divider powered by the supply voltage V_{DD}. But now the idea is exactly the same, the gate has to get connected to something for ac and something else for dc.

So, what we do is the following. Let me show this broken here. This point should get connected to the drain for dc. I connected through a resistor, let me just call it R_G. At the same time, you should also get connected to the signal source for ac. So, I connect it to the signal source through a capacitor C_1. And now we have to make sure that this C_1 is much larger than something and we have this R_G, we have to find out the effect of that and so on. So, what we have done is to use the principle of ac coupling to connect the signal source to the gate source

and the load R_L to the drain source. So, I hope the logic is very clear, if not please replay the lecture and follow the logic once more, it is very important that you understand the logic behind every step of this.

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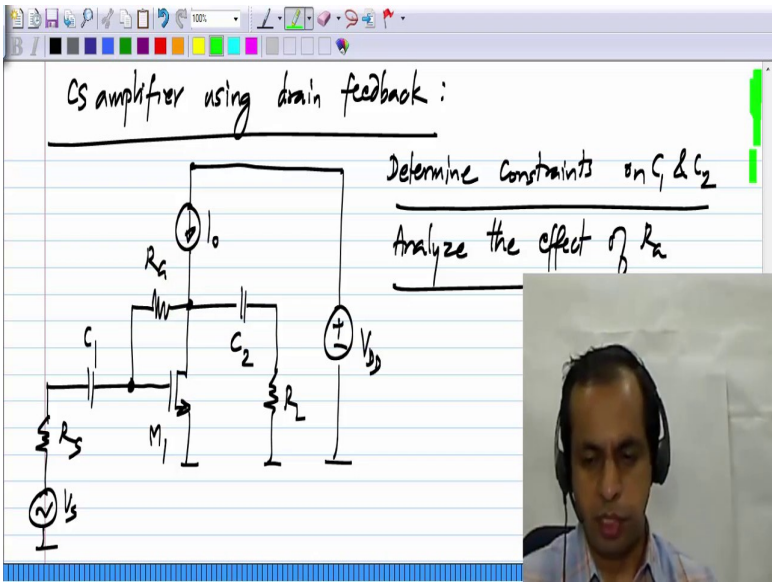

So, the common source amplifier using drain feedback. I will show the complete picture here. So, we have a current source I_0, the feedback to the gate is provided through R_G and that is ok, because no dc flows into the gate, so there will no dc voltage drop across R_G. Earlier, when we were coming up with the biasing arrangement, we had connected the drain directly to the gate, now we connected through an R_G, but it makes no difference at all, because no dc flows through the gate. And the signal source is connected to the gate source via C_1, the load resistance R_L is connected to the drain source via C_2. So, this is the topology. Like I said hopefully you understand all the logical steps leading to this.

Now, we have to, of course, go and analyze this use our circuit analysis skills and analyze the effect of everything. So, we need to determine constraints on C_1 and C_2 just like before. Also, we have to analyze the effect of R_G, because R_G is not a component that is in the basic common source amplifier. So, if you look at this, this is the basic common source amplifier, it has the transistor, signal source and load; that is all. The R_G is something extra, it is similar to the bias resistor we have in the original common source amplifier topology, we had R_1 and R_2 on the gate side, and drain bias resistor R_D, and we analyzed the effect of that and so what happens. So, similarly we have to do it here, we have to find the effect of R_G and see what is

the good value so that it does not significantly or adversely affect the common source amplifier.