

Analog Circuits
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Module - 02

Lecture – 18

Let me copy over this circuit. Again, now you evaluate V_o by V_{GS} , you can think of this circuit as producing some V_{GS} because of V_s and this V_{GS} produces some V_o . The current that flows here is of course, $g_m V_{GS}$ and what we want is the voltage across R_L . Then you have this current division between this resistor and this branch. So, that current is given by R_D divided by R_D plus the impedance of R_L and C_2 in series plus, so that is the current that is flowing in this in the upward direction. So, the actual voltage across R_L , V_{naught} is negative of this, times R_L , which can be written as $-\frac{g_m V_{GS} \times j\omega C_2 \times R_D \times R_L}{1 + j\omega C_2 (R_D + R_L)}$.

Again, now assuming that C_2 must behave like a short meaning, what do we mean by that we have evaluated V_{naught} . When we say C_2 must behave like a short, what we mean is this value of V_{naught} must be the same whether we have this capacitance C_2 here or we have a short circuit. And you see that if this number here, $\omega C_2 (R_D + R_L)$ is much greater than one then you can neglect this one here, because this imaginary part has much greater magnitude. And then this $j\omega C_2$ will cancel off, what will we get $R_D R_L$ by $R_D + R_L$, that is R_D and R_L appear in parallel across this controlled current source. So, this is the condition that we need. This is as far as the output voltage is concerned.

Now, you can also relate these two, the other thing I said earlier how to evaluate this is to identify the capacitor and the resistance across it. You null the source, you set V_s equal to zero, this V_{GS} also becomes zero, because there is no V_s driving this, this V_{GS} becomes zero. And this $g_m V_{GS}$ also becomes so that means this becomes an open circuit. So, what do we have, all we have is a capacitor C_2 and R_D and R_L . So, across the capacitor C_2 , you see the series combination of R_D and R_L and that is what this is saying. If I rewrite it differently in terms of the reactance, one by ωC_2 , the

reactance of the capacitor must be much smaller than the resistance across it, which is $R_D + R_L$, so that is how we can choose C_2 .

And as before, you calculate the constraint on C_2 , C_2 must be much larger than a certain capacitance C_{naught} . And if you, in the practical circuit use about ten times C_{naught} that is usually good enough. Now, this is perfectly all right as far as V_{naught} is concerned, but there could be a slight problem with this particular choice of C_2 that I will show. Let us evaluate this V_D , which appears between the drain and source of the transistor that is the incremental V_D . Everything here is incremental, this is the incremental equivalent circuit. If I do that, what is that, this V_D is nothing but, this current flowing into the parallel combination of R_D and this series branch.

So, V_D by V_{GS} equals minus g_m times R_D times R_L plus 1 over $j\omega C_2$ divided by the sum of everything R_D plus R_L plus 1 by $j\omega C_2$. Now, previously we had only R_L in the numerator for V_o , if you look at this expression. So, the bottom line is, the drain voltage magnitude will be greater than the output voltage magnitude. And this is especially so if R_D is very large. So, let me rewrite this as minus g_m one plus $j\omega C_2 R_L$ plus $j\omega C_2 R_D$ plus R_L . So, now you see that you have this extra factor one here, if R_D is very large the drain voltage can become much larger than the output voltage. As far as the incremental equivalent circuit is concern, there is no problem at all. If you satisfy the earlier condition, you will get the value of V_{naught} , which is minus g_m times R_D parallel R_L times V_{GS} .

But, in practice, you also do not want the voltage across the transistor to become very large, because it is after all the non-linear device and that will cause nonlinearities. So, in this case, you have to satisfy both conditions that is you want the voltage here to be equal to V_o , not much larger than V_o . In this case, you have to satisfy both conditions, you want this number to be much more than one, and this number to be much more than one, that is $\omega C_2 R_L$ to be much more than one, and ωC_2 times R_D plus R_L to be much more than one. And you clearly see that this is the stronger condition as far as C_2 is concerned. And if R_D and R_L are about the same magnitude, these two are about the same. If R_D equal to R_L , this is two times that, so it is not a big problem, but if R_D is ten times larger than R_L , what can happen is it could satisfy this condition and not that one.

So, typically on the output side, you try to satisfy this condition that is $\omega C \gg 1/R_L$ being much more than one. The reason I went through all of these calculations is to make sure that this is not for the output voltage, the output voltage will come out just fine, even if you satisfy this one. This is just to make sure that the drain source signal voltage equals the output voltage. So, I hope you understand exactly how these criteria are arrived at. Essentially, it is like evaluating time constants, which you would have done in basic electrical circuits course. As I said please revisit that you need to know sinusoidal steady state analysis or phasor analysis in order to do these things fluently.

And once you do that, once you understand these things for first order circuits, which is what we most often encounter, the criterion is really easy. You identify the capacitor, you identify the resistor across it and make sure that the capacitive reactance is much more than the resistive, the capacitive reactance is much smaller than the resistive reactance.

Now, one last thing when we have multiple capacitors, what do you do, the easiest thing is, I mean you could calculate the entire transfer function with multiple capacitors all together, it can lead to very messy expressions. So, what you do is the following, you take one capacitor at a time, and for calculating the value of that capacitor while doing that assume all other capacitors are shorts. This way you will only have to consider first order circuits. And each of this is each of this is only going to give an inequality, it says that capacitor has to be much larger than something, so you make it ten or twenty times larger than that and everything will be fine.