

**Analog Circuits**  
**Prof. Nagendra Krishnapura**  
**Department of Electrical Engineering**  
**Indian Institute of Technology, Madras**

**Module - 02**

**Lecture – 16**

This is the final equivalent circuit assuming large capacitors, and this basic amplifier, this is known as common source amplifier, because MOS transistor has gate, source, and drain. And the input is applied to these two points; this  $V_s$  somehow appears between these two or fraction of it will appear. So, the input is applied to gate source, and the output is taken between the drain and source terminals. So, given this the source terminal is common to the input and output that is why it is called a common source amplifier. And this is the very basic type of amplifier, you can build with the MOS transistor.

Now, let us analyze this; it is quite easy that is the common source amplifier. And what do we have here, we have  $V_s$ ,  $R_s$  and this whole thing can be replaced by a single resistor, which is  $R_1$  parallel  $R_2$ . And you can see that these two resistors form a voltage divider driven by the source  $V_s$ . So, this voltage here, which is  $V_{GS}$ , this is equal to  $V_s \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_s}$ , quite easy. And this is approximately equal to  $V_s$ , if  $R_1 \parallel R_2$  is much more than  $R_s$ . And for this condition to be satisfied, you know that both  $R_1$  and  $R_2$  have to be much more than  $R_s$ . So, this component here, remember this  $R_1$  and  $R_2$  these are there for biasing the transistor, biasing the gate of the transistor. And they do have some effect on the circuit. The actual gate source voltage applied is smaller than the input voltage  $V_s$ , but you can fix the situation by making  $R_1$  and  $R_2$  very large.

And fortunately, you can do that, because this  $R_1$  and  $R_2$  forms a voltage divider for this supply and it supplies the gate of the transistor. Now, if the gate draws some current that will change the voltage here. Remember, the open circuit voltage here, because of the voltage divider is  $V_{DD} \frac{R_2}{R_1 + R_2}$ ; but if some current is drawn from it, the voltage will be different. So, you can analyze the circuit for yourself and then see, please use superposition to analyze this and convince yourself that is the case. You know the open circuit voltage here, that is  $V_{DD} \frac{R_2}{R_1 + R_2}$ . Now, we imagine that there is some current  $I_{gate}$ , the gate current was being drawn

from it; what will be this voltage, you please calculate that and see for yourself that it changes. But in our case,  $I_G$  is zero, no current is drawn, so this voltage will not change at all, regardless of the value of  $R_1$  and  $R_2$ . You will see that if there is a gate current then you cannot make  $R_1$ ,  $R_2$  arbitrarily large, but now you can.

So, that way although these two resistors  $R_1$  and  $R_2$  have some effect on the circuit, you can ignore that effect by making  $R_1$  and  $R_2$  very large. And there is no other harm done by making  $R_1$  and  $R_2$  very large, so that is for the input side. Now, what is the current flowing here, it is simply  $g_m$  times this voltage. I will assume that we already satisfied this condition, so this voltage here is approximately equal to  $V_s$ . So, this voltage here, this is  $g_m V_s$ , this current here this is  $g_m V_s$ . What is the voltage across this, this current goes into the parallel combination of  $R_D$  and  $R_L$ . So, the voltage in this polarity is given by minus  $g_m R_D \parallel R_L$  times  $V_s$ . So, you can see that originally I wanted a gain of minus  $g_m R_L V_s$ , that was my intention.

Now, this  $R_D$  has appeared in parallel with  $R_L$ , and you know that the parallel combination is going to be smaller than  $R_L$ . So, this gain is going to be smaller in magnitude compared to the original gain; so this  $R_D$  also ends up reducing the gain. This  $R_1 \parallel R_2$  also reduce gain, because this ratio is smaller than one, but you could make this much larger than  $R_s$  and get around that problem. Here also if you make  $R_D$  very, very large, then  $R_D \parallel R_L$  will be approximately equal to  $R_L$ , and we get the same gain as before. In other words, this current goes into parallel combination of two resistors, if  $R_D$  is much larger than  $R_L$ , almost all of this current will go into  $R_L$  that is the idea. This  $R_D$  does not draw any current.

But what does this do, if you make  $R_D$  very, very large. Let us go back to the full circuit. Here we have calculating the operating point; we know that the voltage across this, what is it. Let us assume that the transistor is in saturation, so it is carrying a current two hundred microamperes, in general some  $I_{D0}$ . And in the operating point condition that  $I_{D0}$  will flow through  $R_D$ . So, the voltage drop across this is  $I_{D0}$  times  $R_D$ .

And the voltage drop across the transistor  $V_{DS}$ , the operating point  $V_{DS}$  equals  $V_{DD}$  minus  $I_{D0}$  times  $R_D$ . Now, you can see what happens, if  $V_{DD}$  is fixed, if the supply voltage is fixed, then if you go on increasing  $R_D$ , this  $V_{DS}$  will go on reducing, the operating point  $V_{DS}$  will go on reducing. And we know that  $V_{DS}$  has to be greater

than  $V_{GS} - V_T$  for the transistor to be in saturation. So, for a fixed  $V_{DD}$ , increasing  $R_D$  drives the transistor into triode region. Alternatively, if you want to maintain a fixed  $V_{DS}$ , let say we wanted  $V_{DS}$  to be fixed, we decide that you want to have a certain  $V_{DS}$ , and you want it be fixed then increasing  $R_D$  requires an increase in the supply voltage  $V_{DD}$ , because  $V_{DD}$  will have to be whatever  $V_{DS}$  you choose plus  $I_{D0}$  times  $R_D$ . So, because of these reasons, the drain bias resistor  $R_D$  cannot be increased indefinitely, because you do not have unlimited supply voltage, you have to live with some supply voltage that is given by the battery.

So, you cannot increase  $R_D$  indefinitely, which means that you have to live with this reduction in gain. This part the reduction in gain due to this is easy to solve; the reduction in gain due to this is not. So, these are practical things that come about, we have to setup the right operating point in the transistor. We do need  $R_1$  and  $R_2$  and also  $R_D$ . And they do have some effect on the operation of the amplifier that is that they end up reducing the gain. As far as the gate bias resistors are concerned, you can make them very large and reduce this effect; and as far as the drain bias resistor is concerned, we cannot fix very easily, because that requires increase in the supply voltage. Otherwise, you will drive the transistor into triode region, so that is not that easy. When we have this prototype common source amplifier, we have to live with this short coming, and this  $R_D$  usually will end up being comparable to  $R_L$ , so you will have some reduction in gain.

What this really means is, if you want to certain gain, you have to also take into account  $R_D$ , while designing it, so that is the summary of the common source amplifier including all the details. So, this should give you a pretty good idea of a first of all if you see a new circuit, how to start analyzing it, and also all the practical constraints that come about. Although our functionality is the small signal incremental functionality and we wanted a gain of minus  $g_m R_L$ , because of the biasing components we can have some reduction in gain or some effect in different circuits. All these have to be analyzed.