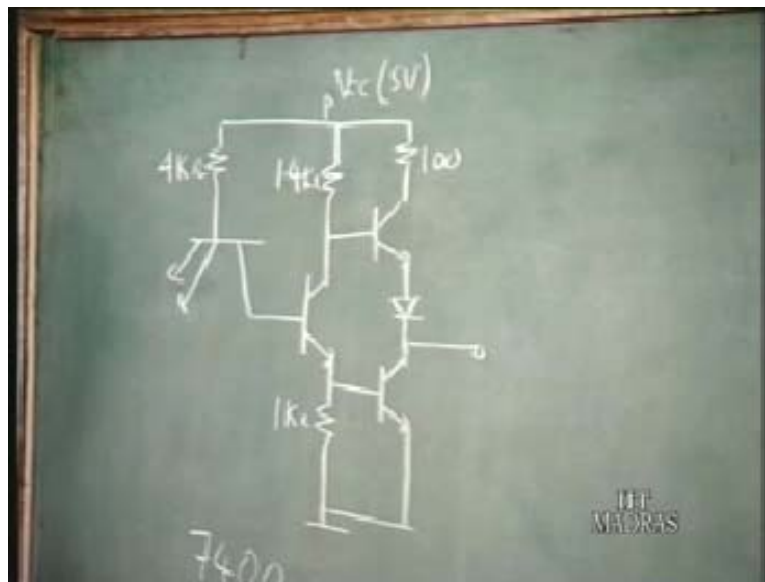


Digital Integrated Circuits
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Lecture-9

Quantitative Discussion on Standard TTL Circuits

Today we shall continue our discussion on this 7400 TTL gate and draw the circuit once again. This is the earliest form of the TTL gate and it is important to understand the circuit how it works and then once we understand this we can look at the modifications. We can very easily understand the modifications in the later stages in the more advanced versions of this gate. So this TTL always uses 5 volt power supply, these are the resistance values, this is the TTL NAND gate 7400.

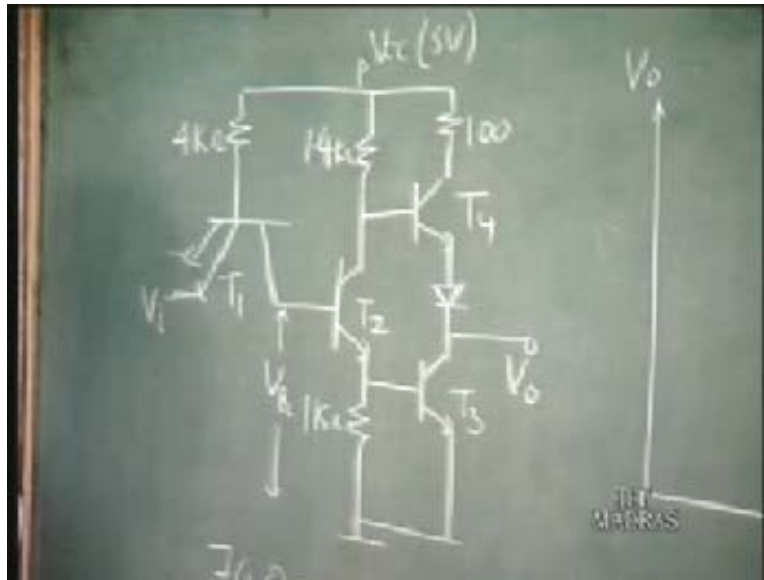
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So what we shall do first in today's class is we shall obtain the input output characteristics of such a gate. This is the output point and we shall take one of these inputs as the input to the circuit. Before actually going into the input output characteristics, the better way to do this is to consider this input at the base of T_2 , of the transistor T_2 and obtain the characteristics of the output voltage versus the voltage at the base of T_2 that is V_o , V_{B2} characteristics. Once we do that then we can very easily get the input output characteristics by obtaining the drop across, if you know what is the drop across the T_1 transistor.

Now let us see what is the characteristics like. When V_{B2} is say zero volts then what happens to T_2 ? T_2 is off obviously because the base voltage is small and if T_2 is cut off T_3 will also be cut off because there is no emitter current for this and if there is no

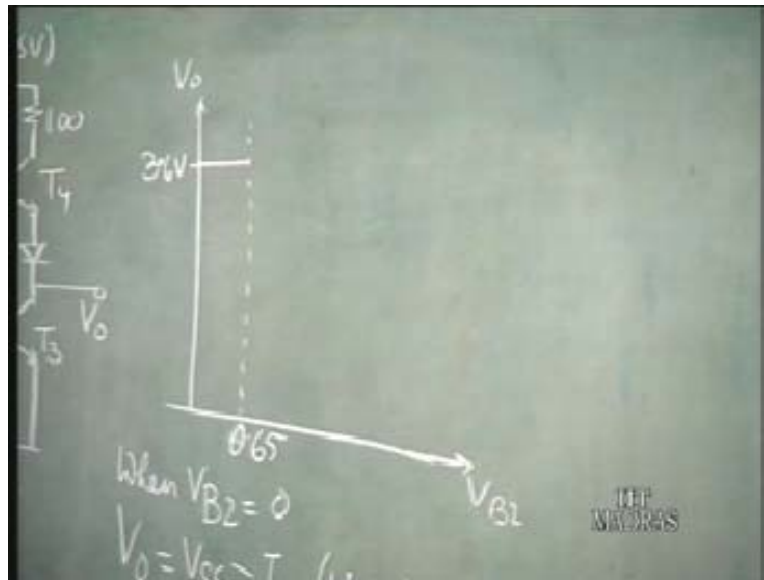
emitter current T_3 cannot have any base current, so T_2 and T_3 is cut off and what about T_4 because there is a base current for T_4 , T_4 will be on.
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What is going to be the output voltage? Now the output voltage will be, when V_{B2} is equal to zero, V output would be equal to V_{CC} minus I should call this I_{B4} , this current which is the base current of T_4 ; I_{B4} into 1.4 kilo ohm minus V_{BE4} minus one diode drop. We know all this, V_{CC} we know 5 volts these we can assume to be around 0.7 volts . Now this voltage drop if you assume say that the load is it depends on the load current actually, how much current you are actually drawing which is the emitter current of the transistor T_4 . So if you assume that this load current is one milli ampere and if the beta is 50 of this transistor then the base current is around 20 micro ampere and 20 micro ampere into 1.4 kilo ohm would be 0.02 into 1.4 that is its less than 0.1 volts .

So we can almost neglect this term. If you assume 0.7 volts each this is almost equal to 3.6 volts . So when V_{B2} is equal to zero, output voltage would be around 3.6 volts . Now how long does this output voltage remain at 3.6 volts ? As long as this situation prevails, we can say that this situation is going to prevail as long as T_2 is cut off. Now if we say that the base input voltage at which T_2 starts conducting I mean the base currents starts to flow at T_2 is around say 0.65 volts or something. Then we can say that till V_{B2} is 0.65 volts , this output voltage will remain at 3.6 volts . Then we can draw like this, this is point 0.65 volts , so the same situation prevails. So we can say I just write it here, when V_{B2} is less than 0.65 volts , T_2 and T_3 are off and T_4 is on and that is why you get V output is equal to 3.6 volts . Now what happens when it exceeds 0.65 volts say, when this input exceeds 0.65 volts , V_{B2} .

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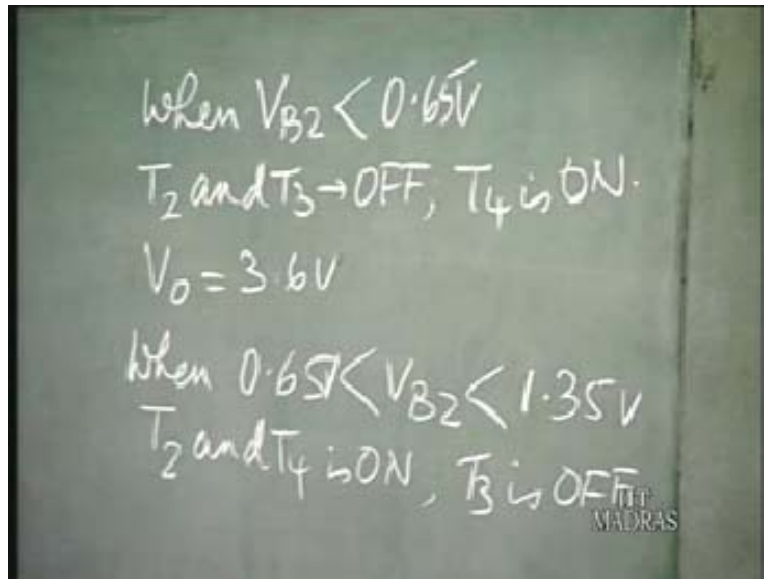
This transistor T_2 is going to start conducting and when T_2 starts conducting, this part of the circuit which I called it the face splitter part, this behaves as an amplifier with a gain of minus R_C by R_E you know that, an amplifier. So that is 1.4 by 1 that is 1.4. So the voltage at this collector point is going to fall, is going to have a gain of minus 1.4 with respect to the base voltage. So as the base voltage keeps on increasing, this voltage falls by 1.4 times that and since this point here is basically the emitter follower point of this transistor, this is also going to follow. That is the output voltage here is also going to have a gain of minus 1.4 with respect to V_{B2} because you know this voltage is 0.7, 0.7 they remain almost constant, they do not change.

So as we go on increasing the base V_{B2} , this output voltage is going to fall with a slope of minus 1.4 and how long is that going to happen. Till the point, till T_3 starts conducting. Now what is this voltage range in which T_2 is on but T_3 is off? Now as you go on increasing this voltage what is going to happen is, this voltage is falling but this voltage is increasing. That is the base voltage of T_3 or the emitter voltage of T_2 that voltage is increasing because that is the emitter follower point. So if we say 0.65 is the cut in voltage, so when this voltage becomes 0.65 that is at the base of T_3 , this T_3 is going to turn on.

Then if you say that at point T_2 , the base voltage of T_2 is 0.7 volts because it is conducting this is 0.7 volts V_{BE2} is 0.7 volts then we can say that V_{B2} is 1.35 volts

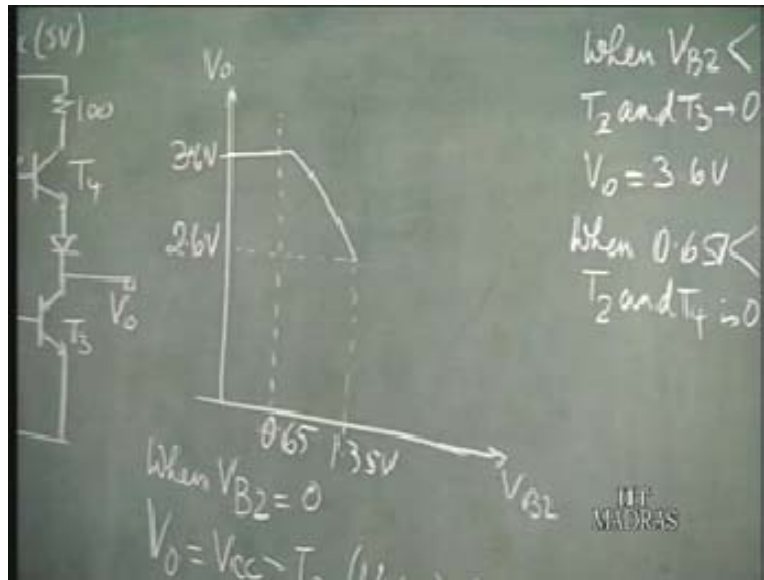
because this is 0.7 and at the base of T_3 is 0.65. So when I can write here, when V_{B2} lies between 0.65 and 1.35 volts, T_2 and I will say T_4 is on, T_3 is OFF. So at this range what is the output voltage? The output voltage falls with a gain of minus 1.4.

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This range, when V_{B2} becomes 1.35 volts here, this is going to fall. So this is 0.7 volts difference if the slope is minus 1.4, this would be around one volt so this is 0.26 volts.

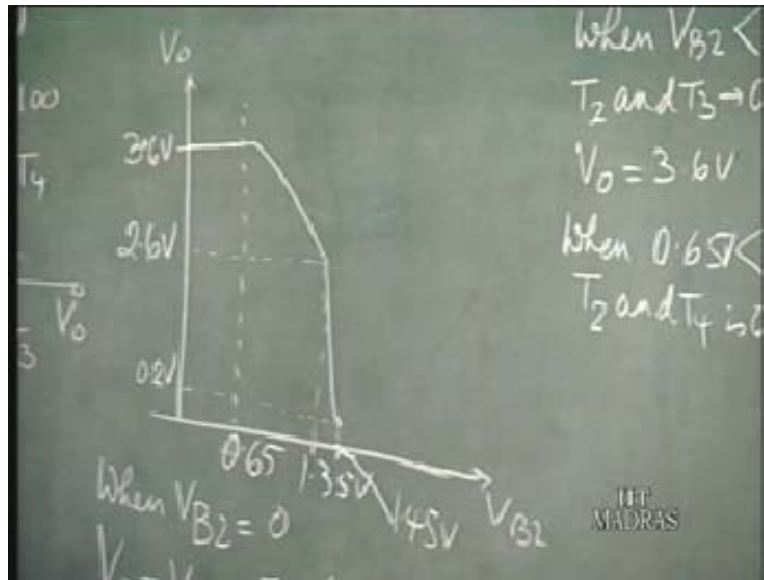
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Now what happens? This has become 0.65 volts and now if you go on increasing V_{B2} even further, this output voltage will fall with the slope is going to increase even further. Why, because if you look at this amplifier now, this input of this transistor is coming in parallel with this one kilo ohm and so what happens is effectively the emitter resistance is going to be reduced and so the slope is going to be increased. So the output voltage is going to fall more sharply and so both T_2 and T_3 is conducting.

So what is going to happen is ultimately because T_3 gets its base current from the emitter current of T_2 , mostly part of it is of course bypassed but of course most of it flows in as base current of T_3 . T_3 is going to go to saturation before T_2 because the base current is much larger in the case of T_3 because it is derived from the emitter current of T_2 which is I mean it's a large base current. So T_3 in fact goes to saturation before T_2 , so around V_{B2} is equal to 1.4 volts, 1.45 I should say if you say that at saturation V_{BE} is 0.75 volts, 0.75 and 0.7 so at around 1.45 volts, T_3 goes to saturation and when T_3 goes to saturation what is the output voltage? Its 0.2 volts so there is a very sharp fall you can see. It actually goes down like this, at 1.45 volts this is 1.45 volts the output voltage has reached 0.2 volts.

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This is 0.2 volts and now of course if you go on increasing V_{B2} even further, this at 1.5 volts if you assume that 0.75 volts is the base emitter voltage at which the transistor goes to saturation, at 1.5 volts T_2 also goes to saturation. So it keeps on like this but you must understand the fact that you are not applying V_{B2} there is no external voltage source and V_{B2} cannot exceed something like 1.5 volts because it would mean that the base emitter drop of a forward bias junction is very high which is not possible again as we said. If you plot the V output V_{B2} characteristics, you must have to truncate it here because this voltage cannot go more than that. So what happens, the V output V_{B2} characteristics? So this is this characteristics.

Now what we are going to do is we will try to translate this V_{B2} axis, you would basically like to draw the corresponding V input axis and see what are these values on the V input axis. So what I mean is that when V_{B2} is 0.65 what is V_I ? When V_{B2} is 1.35 what is the value of V_I and then we will have the input output characteristics. So basically we will have to understand the state of this transistor T_1 that is the multi emitter transistor here. When V_I is quite large I mean when the input voltage is quite high I should say what is the state of this transistor?

This transistor is acting in the active inverse mode, you know that we have already discussed and this base current flows into T_2 of course and this V_{B2} will be at around 1.5 volts and this output voltage is going to be 0.2 volts. When V input is quite large, you have output voltage as 0.2 volts. Now suppose you are reducing V input from a very high value, what we want to know is at what value of V_I does this T_2 start coming out of saturation? Because T_2 will come out of saturation before T_3 , because we have already said that T_2 goes into saturation later than T_3 when you are increasing the voltage. So when you reduce the voltage this T_2 will come out of saturation first and then T_3 . So at what value of input does this T_2 come out of saturation? That is when somewhere around this point, this 1.5 is where the transistor goes to saturation. So let us look at that.

Now let us assume again when T_2 is just at the edge of saturation let V_{CE} of this transistor is almost around say 0.3 volts, very close to 0.2 volts say it is 0.3 volts and so and what is this voltage? This transistor is in saturation so here it is 0.75 volts. So what we want to know is that what is the collector current of T_2 or what is the current which is flowing here?

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Handwritten equations on a chalkboard:

$$I_{C(T_2)} = \frac{5 - 0.75 - 0.3}{1.4K\Omega}$$

$$= \frac{4V}{1.4K\Omega} = 2.8mA$$

$$I_{B(T_2)} = I_{C(T_1)}$$

Labels on the left: V_{B2} and $-V_i$. A logo for IIT MADRAS is visible in the bottom right corner.

So if you want to calculate the collector current of T_2 , I_c of 2 under that condition then I_c of T_2 you can write is equal to 5 minus 0.75 minus 0.3, 0.75 is the voltage of the base of T_2 and 0.3 is the drop across T_2 . So that is the drop across 14 kilo ohm resistance. So this is the collector current of T_2 , this is around you can say one volt so its 4 by 1.4 kilo ohm. So this works out to be around how much? 4 volts by 1.4 kilo ohm. So it's around I think 2.8 milli amperes because 0.7 into 1.4 is 1, so it's around 2.8 milli amperes. What is the base current of T_2 which is actually equal to the collector current of T_1 ? This is going to be this divided by beta, so if you assume a beta of 50 say so this is going to be 2.8 milli ampere by 50 which works out to be 56 micro amperes.

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Handwritten calculations on a chalkboard:

$$V_{B2} = \frac{4V}{1.4K\Omega} = 2.8mA$$

$$V_i: I_{B(T_2)} = I_{C(T_1)} = \frac{2.8mA}{50} = 56\mu A$$

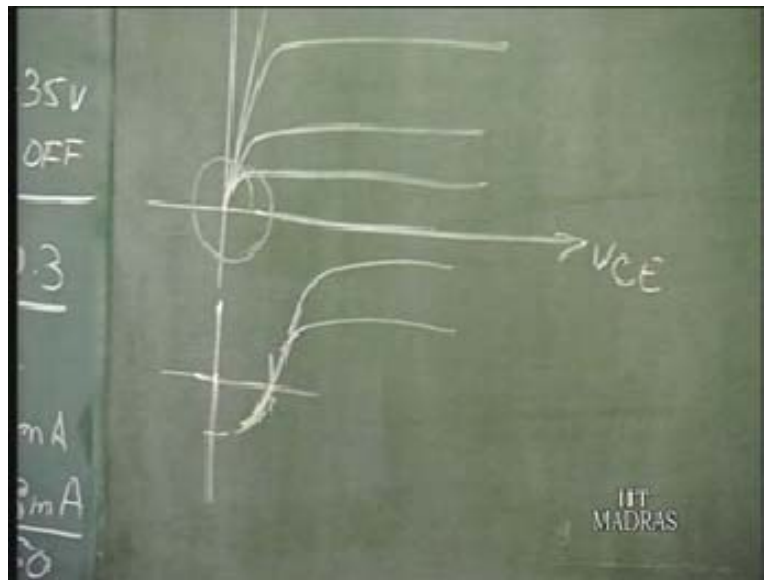
ITT MADRAS

What is happening is at that point of time a current of 56 micro amperes is flowing into the base of T_2 and what is the base current of T_1 ? That is if you assume this is 1.5 volts around 1.5 volts and this junction is also forward biased, so this voltage can at the most be 2.2 volts so you have a 0.7 milli ampere of base current flowing. So in this transistor a base current T_1 transistor, a base current of 0.7 milli ampere is flowing and a collector current that's a reverse collector current basically negative collector current.

Normally in a normal transistor a collector current would flow into the collector in an n p n transistor. So very small negative current is flowing of 56 micro amperes very much smaller compared to the base current and then what happens, if you go on reducing the input voltage even further what is happening is slowly even that 56 micro ampere is going to reduce and finally it will be a zero current, that current goes to zero. The collector current of T_1 reduces and finally goes to zero and this T_2 is cut off. So if you look at this region of these characteristics at this end, when the T_2 is just at the edge of saturation a very small collector current, a negative collector current is flowing and as you reduce the input voltage, what is happening is that negative current goes to zero?

So at what region of characteristics is this transistor operating? You have to recall our discussion on the bipolar transistor characteristics and I had referred to one particular region of the characteristics and said that we are going to come back to it when we discuss TTL. So if you look at the transistor characteristics, we usually draw it like this but I said if you magnify this region, it is something like this. The characteristics actually start off something like this and this region is called the offset region. So this is V_{CE} this is the output characteristics, so in this region I_C is negative. So negative and then slowly it goes to zero so basically I_C goes to zero at a small positive V_{CE} which is called the offset voltage of the transistor and we have also seen the reason for that when we discussed the bipolar transistor.

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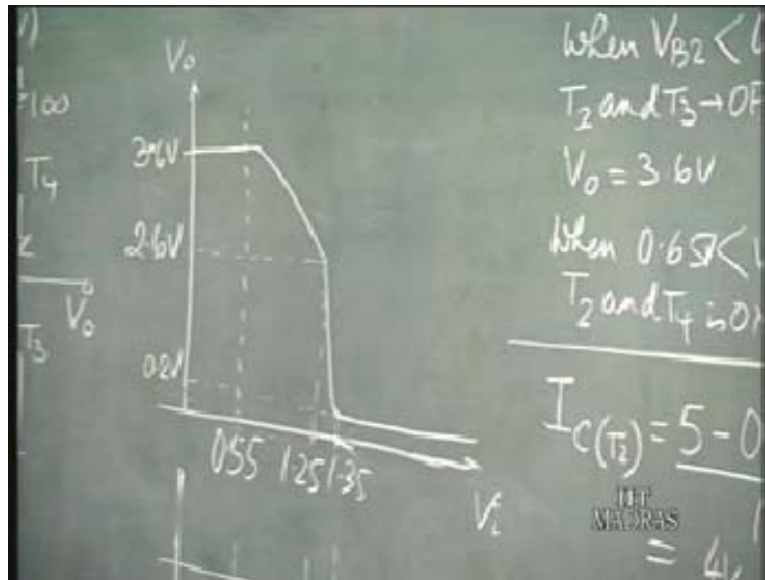


Basically what is happening is it is operating in this region, so small negative current 56 micro ampere which goes to zero. So it is almost confined to a small region here throughout the entire operation of this region, for T_1 it is confined in that region. So approximately we can assume that the drop across the V_{CE} of T_1 is around 0.1 volts along the entire region here, it's a very small voltage around 0.1 volts say. Now if V_{CE} is 0.1 volts for T_1 in this entire range so basically we have to translate or shift this axis by 0.1 volts to get the input output characteristics.

Of course it is going to change by a small amount it's not constant but it's almost a constant it changes by a very small amount because this entire range is very small so it's around 0.1 volts and it goes like this. If you look at it like that it's a very small region. So what you have here is this 0.65 will become 0.55, 1.35 would become 1.25, 1.45 would become 1.35 so on and of course when you draw the input output characteristics you are not constrained here, you can go to high voltages. So basically if I draw the input output characteristics what I am going to do is this remains the same.

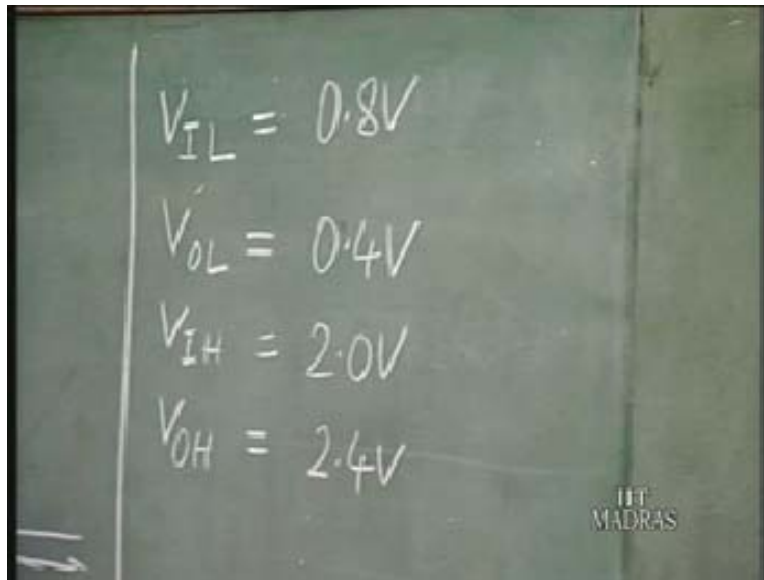
I am just going to make this V_I now, I just make this 0.55, this is 1.25, this is 1.35 and this can go on because as you increase the input voltage, this remains in saturation and the output voltage is 0.2 volts. So this is the input output characteristics of this TTL gate.

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The next thing we shall see is about some further specifications of this gate. Now if you look at the manual of 7400 c gate and look at the different specs of this gate, you will come across the values. These terms we have already defined V_{IL} , V_{OL} , V_{IH} , V_{OH} . you know what they are in terms. V_{IL} the values which are given is V_{OL} is 0.4, this is 0.8, V output 2.4 volts and this V_{IH} is 2 volts. So these are the specifications provided by the manufacturer which means that V output low, the maximum value the output can have when output is low is 0.4 volts and V input low that is the maximum value of the input which will be considered the logic low is 0.8 volts.

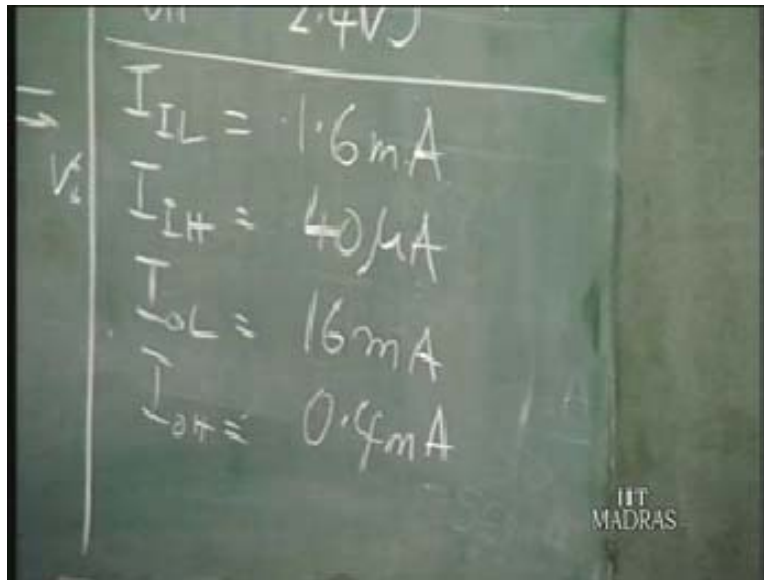
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It is somewhere here 0.8 volts and the thing is they define V_{OH} as 2.4 volts not 3.6 volts because if you define V_{OH} as 3.6 volts, you would have to define V_{IL} as 0.55 volts or even less. Actually if you look at these specifications, you will find that they are conservative in the sense that if you look at the characteristics you can give a better description in the sense that you could say you can put V_{OH} at a much higher value and so on and so forth but why they do is that they manufacture a large number of chips in a batch processing and if they give very stringent conditions they will have to reject lot of their output, so these values are more conservative.

Now they say that V_{IL} is 0.8 volts and V_{OH} is 2.4 volts, it means that if the input voltage is less than 0.8 volts they guarantee output voltage greater than 2.4 volts and if the input voltage is greater than 2 volts the output voltage will be less than 0.4 volts and we see this is going to be satisfied by this characteristics because at 0.8 volts, output voltage is obviously going to be greater than 2.4 and at input voltage greater than 2 volts, output voltage obviously is going to be greater than 0.4 volts. What does this mean in terms of noise margin? The noise margin definition I hope you remember, so the noise margin high noise margin is given by $2.4 - 2$ which means that noise margin high is 0.4 volts and noise margin low is also 0.4 volts that is the another reason for giving this type of specifications because there is no point making one noise margin high and the other low. So these are the one part of the specifications, we will also find another set of specifications which is in terms of current. This is I_{IL} , I_{IH} , I_{OL} , I_{OH} , I_{IL} is the input current when the input is low, for this it is 1.6 milli amperes, I_{IH} is 40 micro amperes, I_{OL} is 16 milli amperes and I_{OH} is 0.4 milli amperes.

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So these are another set of specifications which is given. Now I_{IL} is the input current when the input is low, it is the maximum value. It is the maximum value of the input current when the input is low, so the input current can be at the maximum 1.6 milli ampere.

I_{IH} is 40 micro ampere this is the maximum value of the input current when the input is high. So obviously if you go back at this circuit here, when input is low say 0.2 volts this would be 0.9 volts which would mean actually a current of one milli ampere which is the same as the since this transistor collector current is almost zero. So base current is almost equal to the emitter current, so a current would flow in this way equal to slightly greater than one milli ampere but of course they give a somewhat higher current because in IC technology the resistances cannot be fabricated with such definite values. There is always a tolerance, so if the resistance is much less than 4 kilo ohm the current is going to go up. So they say that the maximum input current, when the input is low is 1.6 milli amperes.

On the other hand when the input is high, this transistor is operating in the inverse mode and the collector current, this behaves as the collector in the inverse mode and the collector current which is flowing is actually beta reverse times the base current which is going to be pretty low because as I said the beta reverse of this transistor is deliberately made very low. So you have a very low input current of around 40 micro amperes. What are these I_{OL} and I_{OH} ? The other two specifications, I_{OL} refers to the maximum load current that the output can sink, so that the output voltage is at logic low. Again I will repeat the definition, I_{OL} is the maximum current that the output can sink, so that the output voltage remains at logic low.

The important thing is that it remains at logic low. What is going to happen is if you sink too much current, again I go back to this circuit here now if it sinks too much current, basically if you connect another gate here say in this NAND gate is connected

to another NAND gates here you have more than one NAND gates. So this is logic low say, now this is the current I_{IL} input low current which is flowing. Where is it flowing into? It is flowing into this gate. So this current is sinking, the output is sinking that current. So if you have more than one fan out, all of them is flowing here. Now if you have too much current flowing in, you see this transistor is in saturation and the condition for saturation is that the collector current should be less than beta times I_B .

Now if you have too much collector current flowing in this transistor, you can come out of saturation and so if it does that then the output voltage is going to rise. So in order to ensure that this transistor is in saturation, you have made this very high effective load but if you have too much current flowing in basically it means that you are reducing the load, the collector resistance effectively which means that the transistor can come out with a saturation. So there is a limit on the collector current which it can sink and the voltage specifications are retained that is the output voltage remains less than V_{OL} .

Similarly I_{OH} , the definition of I_{OH} is that it is the maximum current that the output can source. It is the source current flowing out. When the output is at logic high so that the output voltage is maintained above V_{OH} that is the definition of I_{OH} . That is the maximum current the output can source when it is at logic high, so that the output voltage is maintained above V_{OH} because there is a definition of output high that is the output voltage greater than V_{OH} .

So the manufacturer guarantees that if you do not draw more than 0.4 milli amperes when the output is high, the output voltage will be retained above V_{OH} but if you draw more than that it doesn't guarantee that the output is going to be above V_{OH} . Similarly for I_{OL} if you sink less than 16 milli amperes, output is going to be less than V_{OL} , above that it doesn't guarantee. So there is no guarantee of retaining the proper logic, so this is the input and output current specification and they are very important to understand or the fan out criteria. How many gates can you connect at the output of a particular gate? So you have to look at both the logic low and the logic high, so you have to see for example I_{OL} by I_{IL} so you have to the minimum of...(Refer Slide Time: 38:22). So the fan out I shall write it here separately will be minimum of I_{OL} by I_{IL} and whichever is minimum is going to be is the maximum fan out.

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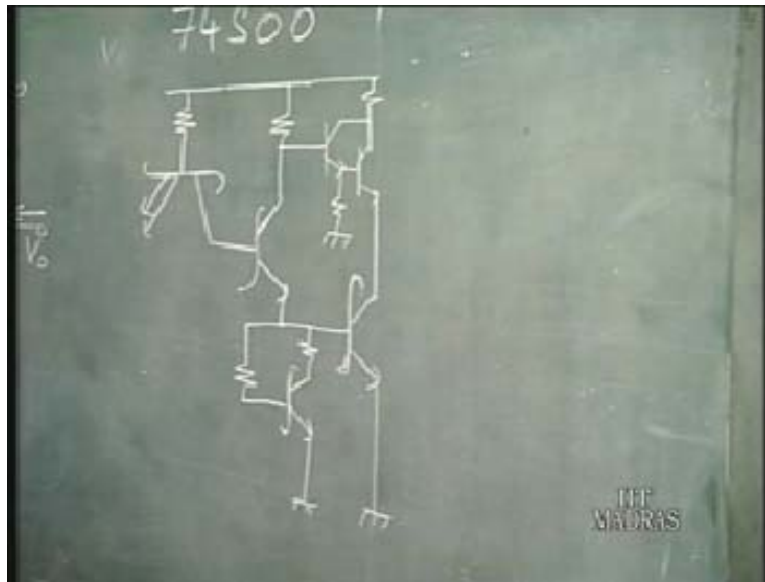
$$F.O. = \min\left(\frac{I_{OL}}{I_{IL}}, \frac{I_{OH}}{I_{IH}}\right)$$

So in this case of course both are 10 so there is no problem but in many cases specially this is very important when you are connecting two different logic families. For example you are having in a circuit, you have both CMOS as well as you are using CMOS NAND gate as well as 7400 series perhaps. Now if you are connecting you must be very careful, whether the CMOS gate can drive a TTL gate. You have to look at these current specifications, you cannot just connect them because the NAND gates and you know that the circuit you just connect them like that, you get it. It will work but it doesn't, you must be very careful of the fan out criteria.

So you have to look at, say if you are connecting NAND gates like this, suppose this is CMOS and this is TTL, so you must see what is the output specifications of the CMOS gate and the input specifications of the TTL gate and you must see how many you can drive. So this is very important, this gives you an idea, this type of specifications when you are connecting any circuit logic circuits using these chips of different logic families.

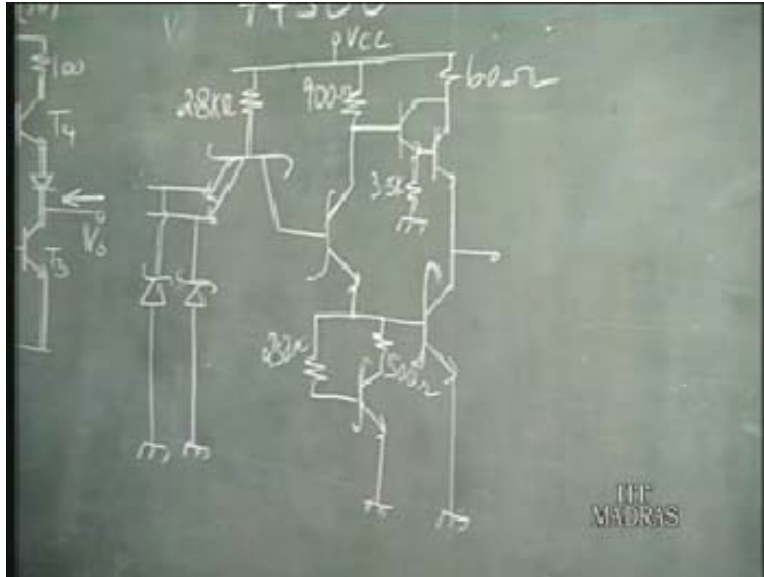
Here of course if you buy TTL, if you have completely one logic family may be they will specify on the spec sheet, you know that maximum fan out 10, we are very sure; but when you have to connect different logic families, you must be very careful. So you must look at this specification sheet, the currents and then only connect; otherwise you may run into problems. So this gives you the complete specifications of the TTL 7400 NAND gate. So I think we have discussed this gate in great detail and we shall now move on to the next gate in this series or shall I say the next series in this TTL gate family, that is the schottky TTL. So this 7400 came out as I said in the mid 60's and then the next improved version of TTL which came out was the schottky TTL series which was the 74 S 00 schottky TTL series, I shall draw the circuit of this gate.

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Then we shall list out the differences between these two circuits and then we shall see the reasons for these changes. This is quite obvious that by the name schottky TTL so this uses schottky transistors. We have already studied what is a schottky transistor, this is the symbol of the schottky transistor. So we will see that this looks like an S, so there are lots of modifications which went into the next version. You can see for yourself now, I hope I have incorporated all of them. These are the values I think 2.8 kilo ohm, this is 900 ohms, this is 250 ohms, 500 ohms, 60 ohms.

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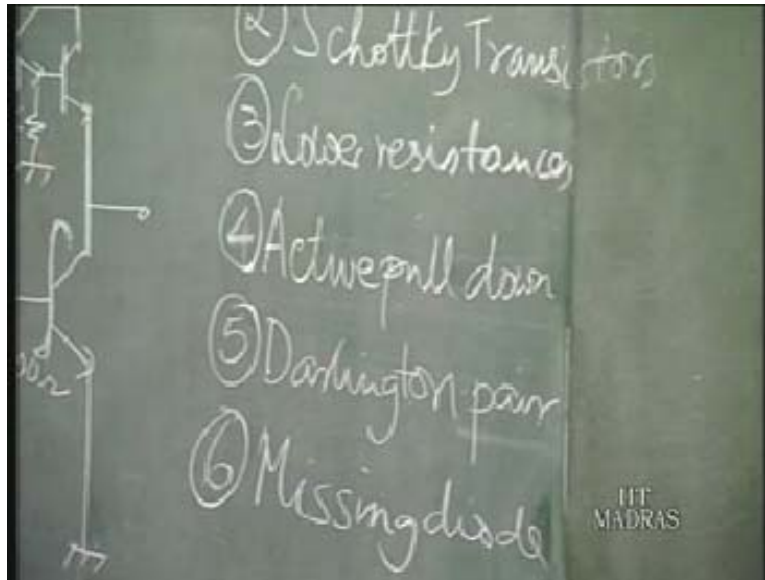


This is the circuit of the schottky TTL 74 S 00 gate NAND gate. Now if you look at the circuit, we can now list out. Actually we have both the circuits on the black board the 7400 here and by the side you have 74 S 00. Now looking at both of them you can now list out the differences, I can give you a hint there are actually 6 major differences. So it's like playing a game having 2 figures and finding out the 6 differences. Can you just point out what are the 6 differences? Yes, there are two diodes at the input, two extra diodes at the input. So they are two schottky diodes, I shall write schottky barrier diodes at input. Then number two, one major difference I should point out is all the transistors, this is also schottky transistor, so all the transistors are schottky transistors except of course one, this need not be a schottky transistor because of the fact that across the collector base junction you have this transistor and since V_C of this transistor is always going to be positive which ensures that this collector to base junction of this transistor is always going to be positive. So it is always going to be in the active region so it's not necessary.

So schottky transistors so that is the next modification. Number three the values of the resistances if you look at them, they are all lower value resistances. The resistance values have been reduced, lower resistances so all the resistances have been effectively slashed.

Obviously I shall tell you that the focus of the schottky TTL is to achieve higher speed and lower resistances give you higher speed, we have already seen that when we talked of a inverter transistor inverter, one way to improve speed is low resistance higher currents which means higher currents. What are we left with? This part of the circuit, so instead of a resistance here at the base of the output transistor you have an active, this is called active pull down, you have an active pull up. So this part instead of resistance you have a transistor circuit here so this is called the active pull down.

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So you introduce what is called an active pull down. Number 5 this one. What is this configuration called, Darlington pair and then what is the remaining one? One diode is missing, missing diode between the two I should say. So these are the six major differences which you see between the two gates. Now what we shall do in the next class, we shall take up each of them, see the reasons for that and how does it improve the performance? So we shall take up this 74 S 00 then we shall go on with the newer series 74 L S which came up later, the further modifications and then even the more recent ones the advanced series of TTL gates which have very good characteristics. So finally will go through the entire range of TTL series gates and with that we shall conclude our discussion on TTL in the next class.