Digital Integrated Circuits
Dr.Amitava Dasgupta
Department of Electrical Engineering
Indian Institute of Technology, Madras
Lecture-7
Specifications of Logic Circuits

Today we shall start our discussion on the different specifications of logic families by which you characterize them. We had already discussed a little bit last class so we shall now go into the details. The first one which we shall take up is propagation delay. What is the propagation delay of logic circuit? Now if you have an input say if you take an inverter say and if the input waveform is like this, the output waveform is going to be something like this.

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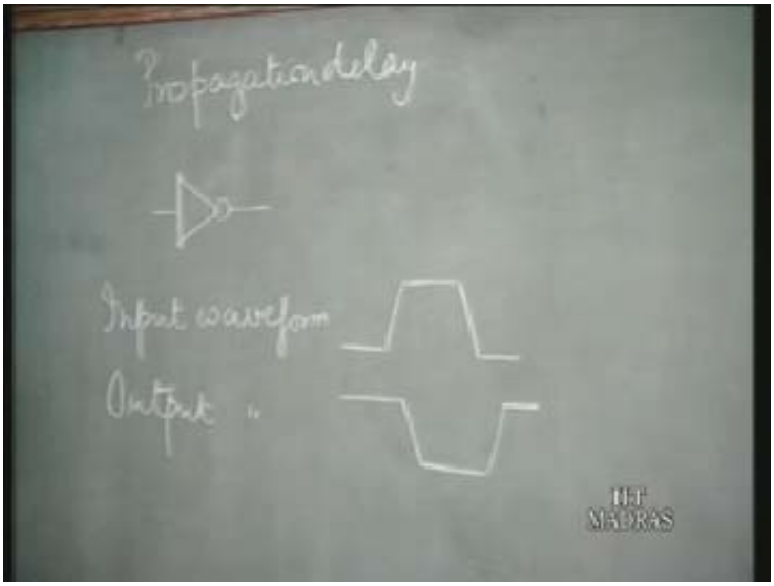

This is how the input and the output varies. The propagation delay is defined as the difference or in time between the 50% points of the input and the output waveform that is this is the logic low and this is logic high. So midway between this logic low and logic high, the instant at which you have, the voltage is at the middle point of the input form and this is for the output waveform. So this difference in time is the propagation delay for a high to low transition. So you should call it tpd_{HL}, HL stands for high to low transition.

Similarly you can have a propagation delay for a low to high transition and these two propagation delays that is for high to low transition and low to high transitions need not be the same, they can be different. Usually the propagation delay of a logic circuit is defined as the average of these two propagation delays.

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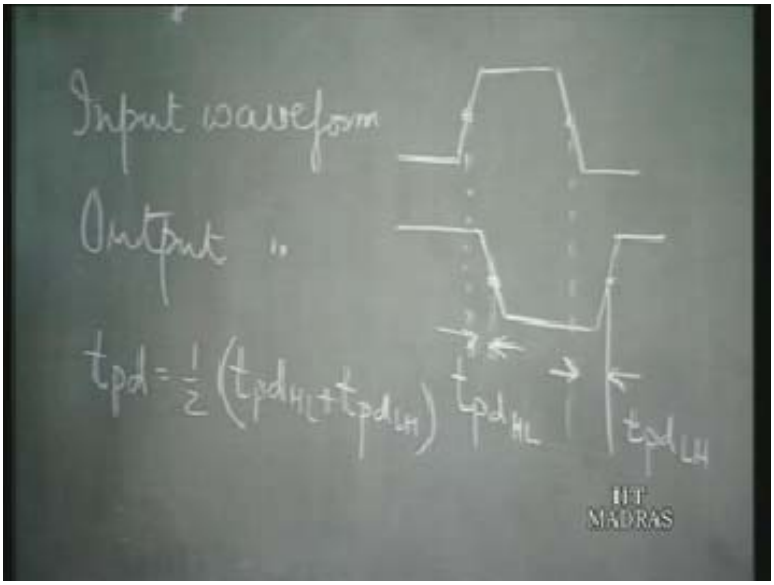

So the propagation delay will be in the average of high to low and the low to high propagation delays. So this is the definition of a propagation delay of a logic gate. Now how to measure it? There is a very interesting circuit to measure this propagation delay which is called the ring oscillator and that is used to measure the propagation delay of any logic gate. The ring oscillator consists of an odd number of inverters. So if you have a NAND gate for example you can connect it as an inverter that is you short the inputs, it behaves as an inverter. So if you have an odd number of inverters say I will draw three inverters like this and you connect it like this and this is called the ring oscillator. Now what is going to happen is suppose this is logic one here, this is going to be zero here, this is going to be one here and this is going to be zero here.

So this is connected here so this one becomes zero and if this one becomes zero here this zero is going to become one and this one is going to become zero and this zero is going to become one. So at each output and again this one is going to be transmitted here. So at each output the voltage constantly toggles between the two levels 0 1, 1 to 0 like that. So if you observe the waveform at any given point or at any input or output of a logic gate, you will observe a waveform like this which is continuously varying, a train of pulses.

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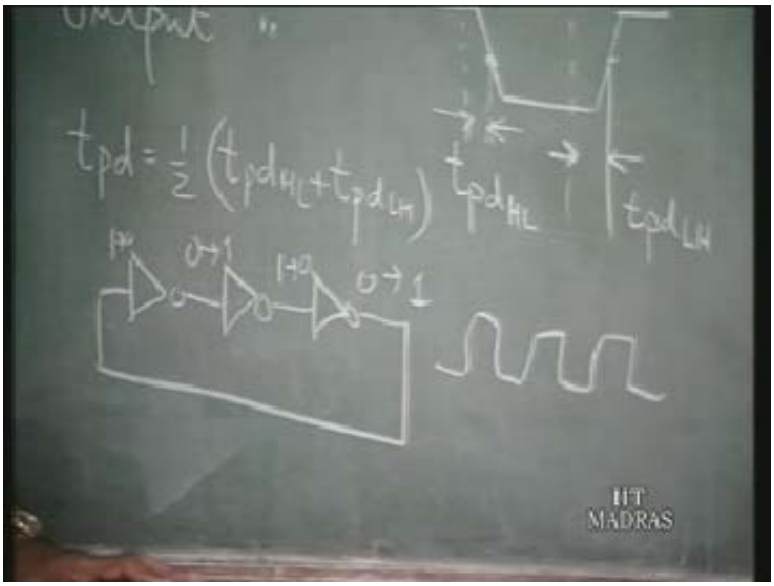

This train of pulses and the frequency of this waveform is going to tell us about the propagation delay because the time required for this one to change to zero is the time required, once this changes from one to zero this change has to propagate through all this and come back here. So once it becomes zero this has to go to one, this one has to go to zero and zero has to go to one then only this changes. So the frequency, the time taken for it to change is determined by the propagation delay and since in each time period you have two transitions, the propagation delay tpd will be given by 1 by 2 Nf where f is the frequency of oscillation or you can write it this way, actually s is equal to 1 by 2 N tpd that is f is the frequency of oscillation, N is the number of inverters and two because in each time period you have 2 oscillation.

Basically the time period of this is equal to twice n tpd, the time period of oscillation is twice N tpd, the propagation delay. So looking at the waveform and knowing the frequency you can find out the propagation delay. In fact this is a very important circuit and is used as a test structure whenever you are developing logic circuit that is you want to know what is going to be the time period or what is going to be the frequency at which you can operate this or the propagation delay of any logic circuit, you usually use this circuit.

In addition to the propagation delay there are two other delays associated with the logic gate what is called the rise time and the fall time. So the rise time is usually denoted by t_r and the fall time by t_f so t_r is the rise time and t_F is the fall time. That is if you look at this, observe this waveform here the time required for this to fall that is the fall time. Usually it is very difficult to find out exactly the time required for it to fall from the logic high to logic low because at these points the transitions are very slow at the edges. So usually it is defined as in terms of the 90% and 10% points.

So the rise time is the time required for the waveform to rise from 10% to 90% value and the fall time is from 90% to 10%. So these are the two other specifications which you may observe if you look at a specification sheet of any logic family. So propagation delay rise time and the fall times and they are very important to know if you are going to make a circuit. So this is about the delays then we move on to the next characteristic which is the power dissipation.

The power dissipation is another characteristic and it is a very important characteristic specially in the present scenario where the trend is to pack in large number of circuits in a given chip as many devices as possible in a given chip. You have millions of transistors nowadays in the VLSI chips, if you are introducing so many devices, the power dissipation is obviously going to go up. So in order to be able to integrate a larger number of circuits, larger number of components the power dissipation has to be brought down somehow.

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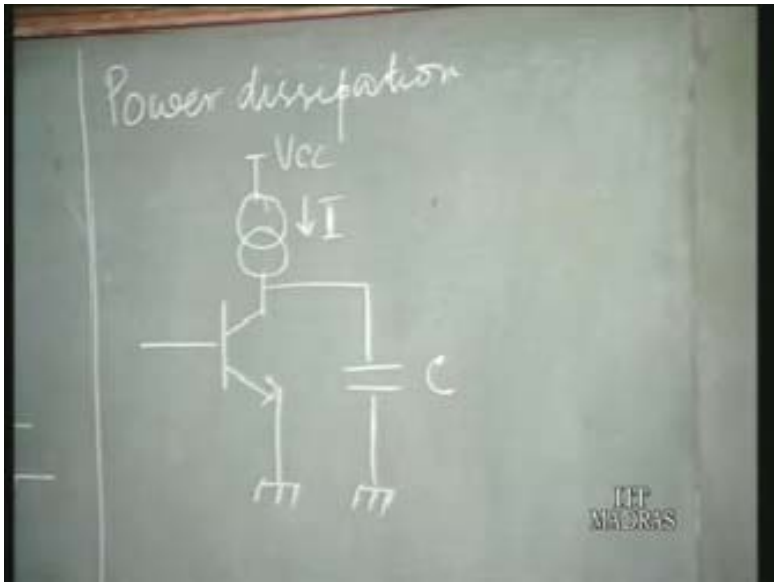

In fact some of the latest microprocessor chips consume as much as 10 of watts of power and if you consider that the voltages or power supply voltages was 5 volts, now

it has come down to 3 volts or so. That means few amperes of currents which is quite a large thing, in the small pins they must be able to carry so much current and that is big constraint. The power dissipation is a very important consideration nowadays and people are looking at ways to reduce the power dissipation. In fact you must have one of the reasons; there are many reasons of course one of the reasons why the power supply voltages are coming down is because of the necessity to reduce power dissipation, so you know that nowadays you hear so much of low power circuits. So lot of research is going on in that anyway. So this is a very important consideration power dissipation, how much power does a gate dissipates that is the basic unit, how much does it dissipate? Just take a circuit like this. Let us consider this circuit, there is a current source I and this is an inverter circuit basically bipolar b j t circuit and this is driving a capacitive load.

Now this is a current source, so if this transistor is on, the current flows into the transistor and this goes to saturation and the output voltage is low and when the transistor is cut off what happens this transistor, the current cannot flow into the transistor it goes into the capacitance and it charges the capacitance, the output voltage goes high. In such a situation if you look at the power dissipation suppose we call this the p_d this is the power dissipation. The power dissipation is given by v_{CC} into I then when you are charging this capacitance with a current i what is the delay? That is suppose the output voltage swing there is a term called the logic swing that is the change in the output voltage that is the difference between the logic low and the logic high suppose it is given by v_L logic.

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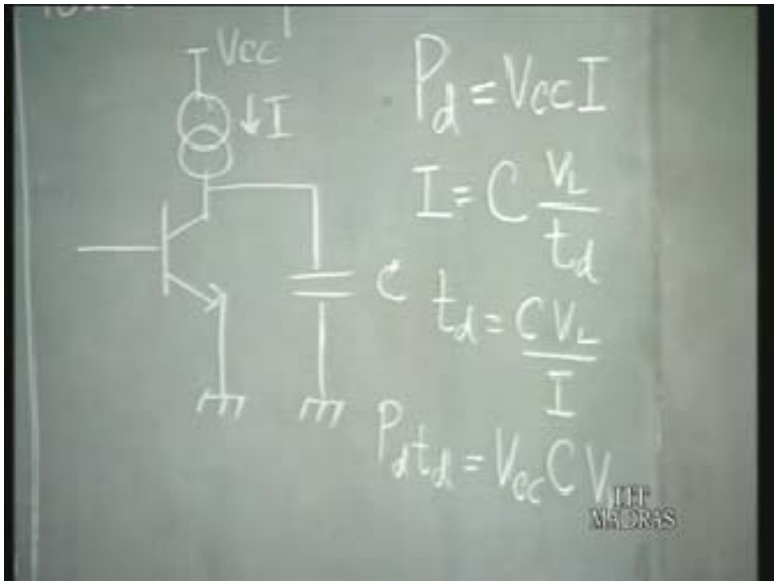

So what is the delay when this capacitance is charged with a current source of value i? When you are charging a capacitance i is equal to c_d v_d. So if you write i is equal to c, so the change in the voltage is v_L which is the logic swing and the delay will be given

by say t_d. So now you can write this as or t_d is equal to c v_L by I then from these two expressions the power dissipation and the delay you can write p_d into t_d is equal to v_{CC} C into v_L. So this expression so this p_d t_d it is an important figure of merit of a logic family, it is called the power delay product and you see that this is independent of the value of the current source. Now in a particular logic family, suppose this is the basic inverter.

Now you can change these value of current by say for example if you have resistance, you can change the value of resistance. Now that is going to affect both the power dissipation and the delay but the power delay product is independent of the current source value and is just dependent on v_{CC} that is the power supply voltage, of course here the capacitive load, the value of the capacitive load and the logic swing. So this is a characteristic figure of merit for the circuit.

In a given circuit you can operate it at different power dissipation levels and delay levels by changing the value of the current. You have a circuit, if you just change the value of resistances for example in the circuit, it will be operating at a different for example if you increase the resistance values, the power dissipation is going to reduce because the current is going to reduce but at the same time the delays are also going to be affected but it is going to affect both the participation and the delay but the power delay product is independent of that. So this is the characteristic of the logic family and so you can operate it at different power dissipation or delay values for example you may have come across some of these curves, this p_d versus t_d.

Now if you plot them on a log scale, these both power dissipation and delay you will get these straight lines indicate constant power delay constants. So that is here you can operate may be a given circuit at this point or this point. You can move along this line that is in a constant power delay product by changing the value of this current source for example but of course you must also remember that this takes into account only a capacitance which is a constant but this is only true when we are operating the circuit, in the view of the last class you must remember that only when the capacitances or the junction capacitance type for a b j t. If you have the diffusion capacitance this capacitance is no longer going to be a constant but again it becomes a function of current.

So when you are operating in the low current regime then only this is true but anyway so this gives us some idea and you can operate the circuit at any of these lines. In fact if you see that for example an ECL would be somewhere here, whereas a TTL would be somewhere here that is although you can operate along this line but in a TTL for example there is a limitation, you cannot go below a particular delay because after that it is no longer going to follow this curve because this capacitance as we have seen in last class, the capacitance is no longer going to be a constant. It is the other capacitances which take up.

For example if you take I square L, you know its somewhere here I square l has a much lower power delay product compared to TTL or ECL. So as a circuit this is a much better circuit but of course there is a limitation as we shall see that you cannot go to very low delays, you cannot operate it at much very high speeds.

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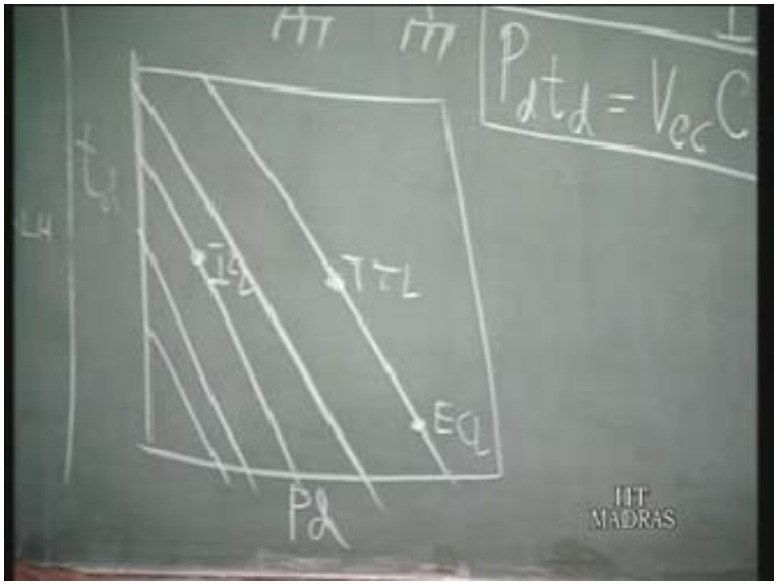

So anyway we shall discuss that in detail. So this power delay product is another important figure of merit or specific characteristic of a logic family. What is the power delay product associated? Now in fact this power dissipation and the speed delays go hand in hand, it gives rise to many interesting considerations. For example let us take a particular logic family where the capacitance which we are looking here is let us say just take two some values 50 feet of error say v_{CC} is 3 volts and v_L is equal to 0.5 volts. Let us consider that many of these chips, the price consideration comes from the packaging.

Suppose you want a one watt package that is package which can dissipate one watt of power. So that is the limitation there, that you must have the power dissipated must be one watt. Now if you go for a ten watt package the price goes up. So you may be want to limit in a particular package so suppose you are going to this particular logic family, suppose you are going to package it in a one watt package and suppose you want to have say there are case one let us say you want to operate it at a very high speed that is say very low delays of say hundred Pico second. So you want to operate the circuits at high speeds. So now the question is for this high speed operation how many gates can be accommodated in a one watt package? How do you do that?

So you have to calculate the power dissipation, so you know that this expression here. The product of the power dissipation and the delay is equal to v_{CC} into v_L. So now what you can find out is you know t_d you know all these things, so you can find out the power dissipation per gate and so how many gates you can accommodate? So I just write it here so C v_{CC} into v_L, if you put substitute all these values what you will get is 0.75 milli watt. So the power dissipation is going to be 0.75 milli watt per gate, if you operate it at a delay of 100 Pico seconds and so if you have a one watt package, so number of gates you can accommodate in the package is one watt divided by 0.75 milli watt. That is 1300 gates in that one watt package.

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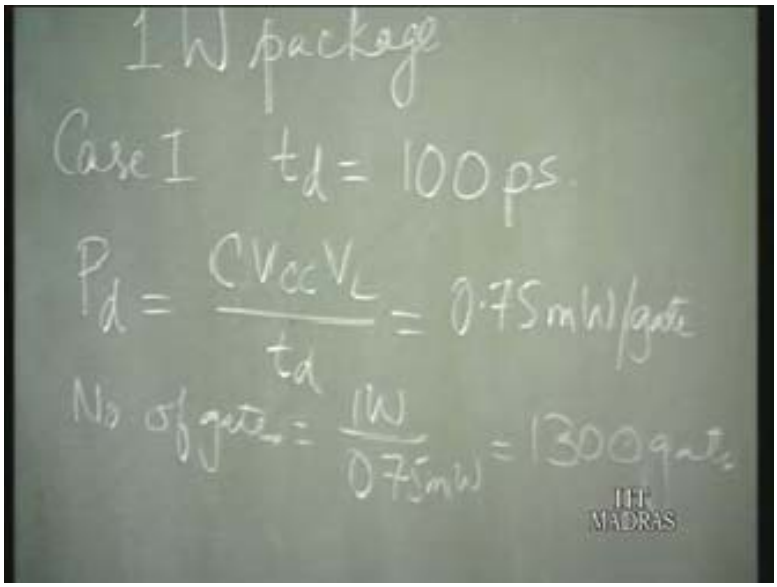

Now suppose in another case you want high packing density, the same circuit you want high packing density. Suppose you want 10 to the power 5 gates per package and you have a more complex circuit. So what is going to be the power dissipation per gate? One watt divided by 10 to the power 5, p_d power dissipation is going to be one watt divided by 10 to the power 5 that is 0.01 milli watt. Now if you write t_d that is again

you put down the values C V_{CC} V_L by p_d which you got here, you will find that the delay is going to be 7.5 nano seconds per gate.

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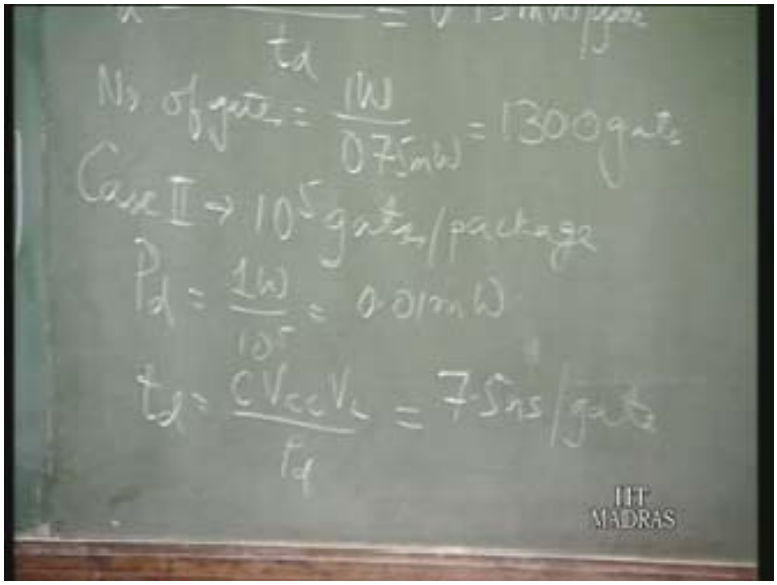

Just put down these values you will get this, so which means that the delay is going to be much higher. So there is always a compromise between the power dissipation and the delay that is what I want to point out that although you talk of power dissipation and delay are separate entities but there is a compromise always. If you want to, you can trade of between these two quantities. So that is about the power dissipation and delay. Then we move on to the next topic that is noise margin that is the third one. The noise margin is also very important characteristic of a logic family and it tells you that how much noise the particular circuit can tolerate, if you are using in a noisy environment.

Now you have seen the characteristic of an inverter, we shall take up again the characteristic of an inverter. So this is the input voltage, this is the output voltage it is something like this. When the input is low, the output is high, when the input is high, the output is low. This is known as the logic swing, the output high and the output low the difference in these values is known as the logic swing. This difference is the logic swing V_L which we have already discussed, this is also an important parameter. Now if a logic swing is high it is true that the noise margin is also going to be high. We shall come to the definition of the noise margin but anyway if the logic swing is high, the noise margin is going to be high but at the same time you can see that the delay also increases in a logic circuit because the output of a gate has to change from the logic low to logic high. Basically you have to charge a capacitor and if you are charging a capacitor through a larger voltage it obviously is going to take more time. If the voltage through which it is charging is less takes less time. So the important thing is that all

these characteristics you know are not independent but they are sort of dependent on one another.

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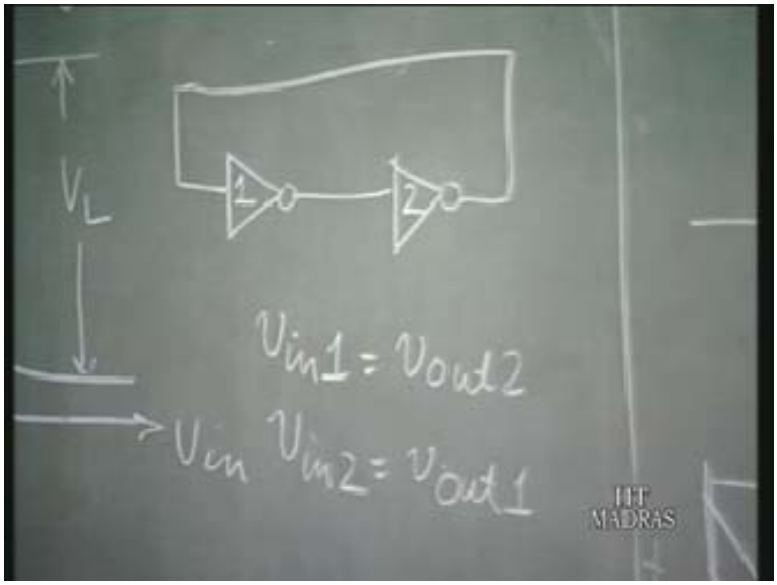

Now suppose you have a circuit like this, you have two inverters we call this inverter one and we call this inverter 2 and so here what you have is you can write v_{in1} is equal to v_{out2} and v_{in2} is equal to v output one. Now suppose this is the characteristic of inverter one, so I will just remove this, this is the characteristic of an inverter one.
Now let us call this v output one and this is v input one. Now this is equal to v output 2 and this is equal to v_{in2}. So if you want to now plot the input output characteristics of the second inverter that is inverter 2. This is the output access, this is the input access so you can plot it like this. This is the same characteristics they are identical inverters, we are just plotting it like this now because this is the output axis, this is the input axis going this way and so now in these two inverters if they are connected like this, the stable points of operation are the points of intersection of these two characteristics. So you see that these characteristics intersect at this point, this point as well as this point. So only at these points v input 1 is equal to v output 2. So this point is actually very unstable because of the very high gain associated with any point because if you have at this point any small perturbation somehow noise or something, it will move away from that point.

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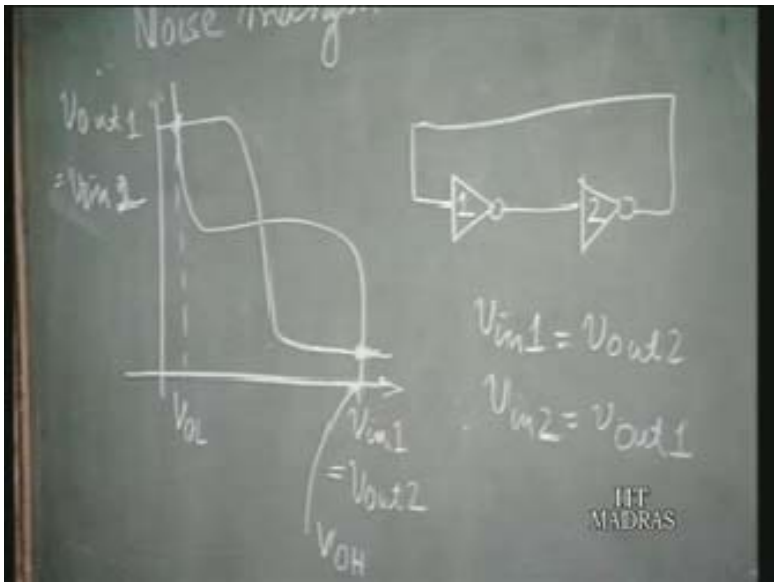

So usually the device operates at this point or this point, so if this point is actually called, this value v output low and this is v output high. So these are the two operating points, this point and this point, these are the two possible operating points of the inverter. Now where does noise come in. Suppose you have a noise source introduced here in between let us call this v_N. Now what is happening is suppose this is low, this is v_{OL} say and so you have the same input to this. Now when the input here is v_{OL} the output is high. Now if the input here it is v_{OL} so here the input to gate 2 is v_{OL} plus v_n and so what is going to happen is the input point to the inverter two actually I should be in this way. Anyway doesn't matter it is the same in whichever way you look at it, I actually should have drawn the noise source here.

So as this noise value increases what you are doing is you are shifting this operating point. So it is moving like this so even if the noise source is this much noise voltage, the output voltage is still equal to this high. This is v_{OH}, this is also v_{OH}, this is also v_{OL}, this is also v_{OL}, this is also v_{OH} if you look at this way it is the same.

When the input voltage changes it is still v_{OH} almost close to v_{OH} but if this input voltage changes by a lot then the output voltage may start to fall and then only it creates problems. Now what is the input voltage up to which it can tolerate? Usually the definition is that where the slope of this curve becomes equal to minus one that is the maximum you can tolerate. When the slope becomes minus one at this point this is called v_{IL} that is the maximum value of the input voltage which is going to be considered as a logic low by this circuit that is v_{IL}. The maximum value of the input voltage which is considered as logic low that is v_{IL} beyond that it is no longer logic low at the input.

Similarly at this end you have another minus slope is equal to minus one point and this is called v_{IH} which is the minimum value at the input which is considered as a logic

high. So this is logic high at the input, isn't it? Normally if you apply this voltage it is logic high but if you the noise source pulls it down. Up to this point it is still considered logic high, after that it is no longer logic high. So it can tolerate this much amount of noise when the input is high.

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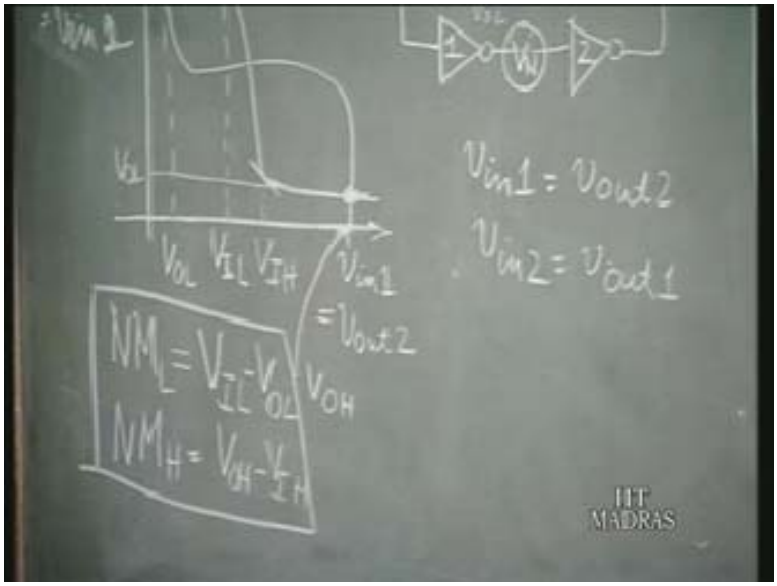

When the logic is low it can tolerate this much amount of noise. So there are two noise margins usually one is for logic low and the other is for logic high. So you have noise margin low is equal to V_{IL} minus V_{OL} and noise margin high is equal to V_{OH} minus V_{IH}. So these are the two noise margins in the circuit. In fact there are other definitions of noise margin also, a more stringent definition as you just pointed out that suppose in this circuit if you go back to this circuit, you have another noise source here and these are equal and opposite noise sources in the sense that when this end is positive, if this goes positive, if this is increasing the input voltage here it is pulling down the output voltage. So this noise source and this noise source further pulls it down, equal and opposite and this is a more stringent condition.

There are two noise sources and both are acting in such a way as to change the state of the particular gate and for that particular condition when you have two noise sources, the noise margin is actually given by what is called the maximum square noise margin, so sometimes you may come across this term. So you must know what it is, the maximum square noise margin. It is called the maximum square noise margin because the noise margin in this case is given by the maximum square that can be accommodated in this region. This drawing is not perfectly correct, the maximum square which you can accommodate here is going to be the same as the maximum square which you can accommodate here because they are sort of identical, from my drawing it is not very clear maybe I should redraw it.

It should go something like this. So here the definition of the maximum square noise margin you don't differentiate between logic low and logic high, it is the same because here in this case if you look at this figure one of the gates will be at logic input will be logic low and the other gate input will be logic high. So it doesn't matter, so that is called the maximum square noise margin that is given by the maximum square and is given by the side of the maximum square which can be accommodated inside this. This value here is called the maximum square V_{MS}, maximum square noise margin this side of the square. So this is another although generally people talk of low noise margin and noise margin high these two noise margins but this maximum square noise margin is also sometimes referred to and that is the definition of the maximum square noise margin where you have two noise sources, sort of aiding each other, helping each other so that even a smaller noise can create more damage. So that is about noise margins and obviously the larger the noise margin the better is the circuit because it can operate at more noisy environment.

In fact the reason why digital circuits have become so important is actually, even if you talk of audio circuits, even such some things like analog that is very much analog like for example audio, amplifiers you have digital amplifiers and many other things which is everything becoming digital nowadays because of the larger noise immunity we can say of digital circuits, because if you look at the circuit you know you can see if you just go back to this you see that even when the input changes by a long margin, the output remains the same. Even while you have lot of noise it does affect the output because here the gain is almost zero, isn't it? The gain is almost zero so the region where you operate a digital circuit know this point or this point the gain at these points are very low almost zero.

So if you have a noise that is almost wiped out there is no effect of noise, only when you come to this part then it becomes important. So that is why the digital circuit is much more immune to noise, it does not easily get affected by noise. So this gives us the idea of the noise margin so what is the maximum noise the circuit can tolerate? Obviously if you want to have a higher noise margin the input output characteristics should be more symmetric. We shall see that as we go about that is basically the noise margin low, it's no point having a very high noise margin high and a very low noise margin low because it is mostly governed by the lower value. So if you have a symmetric input output characteristics that is the transition point I will just go back to that again, this one here.
So another definition I should say this point, if you look at this point which also has lot of significance that is it is called the logic threshold. Logic threshold means at that value, if at this point the input is equal to the output. At this point the input voltage is equal to the output voltage that is it is like this (Refer Slide Time: 44:52). Now when the input is low if you call this logic threshold value here, when the input is lower than the logic threshold, the output is higher than the logic threshold and when the input is higher than the logic threshold, output is lower than the logic threshold.

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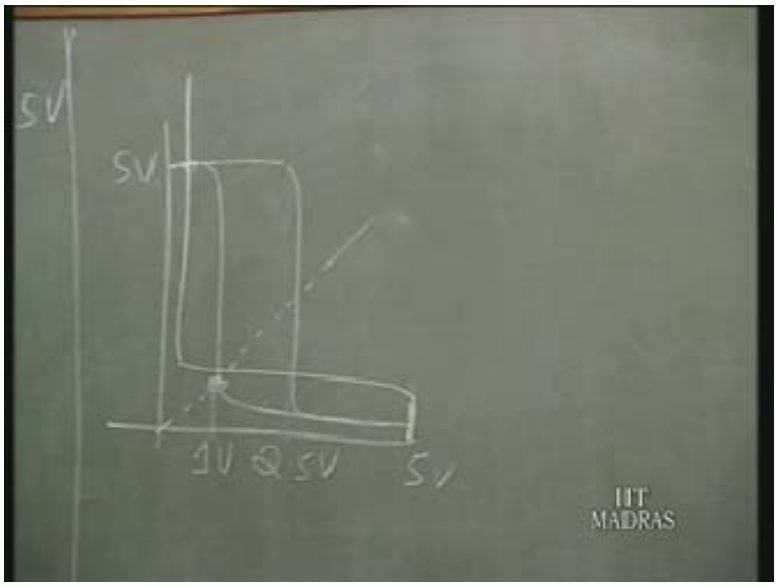

I will just give you an example; I shall just draw two curves, two inverter characteristics. So this is one inverter characteristic so this is another inverter characteristic, now if you draw this, the logic threshold is here for this one. So this is slope is equal to one so v_{in} is equal to v_{out} on this curve and if v_{in} is slightly less than this value then v output is higher than v input because this is inverter and so this is the logic threshold. This logic threshold is much lower here, this logic threshold is much higher here.

Now obviously if you are operating from 5 volts then this is 5 volts. If the logic threshold here is 2.5 volts this is the most symmetric inverter characteristics, this may be 1 volt say. Now if for this one, if I draw the curve like this, as we have drawn previously while drawing the noise margin, you will find that the noise margin low is very small whereas the noise margin high is very large. Again it is the lower value which is important, it's no point having a very high value of noise margin high and having a very low noise margin of very low because you will have in a circuit some gates at operating at output logic low and some at logic high and so if the small value of noise margin, a small noise is going to upset the operation, if you have a low margin of low.

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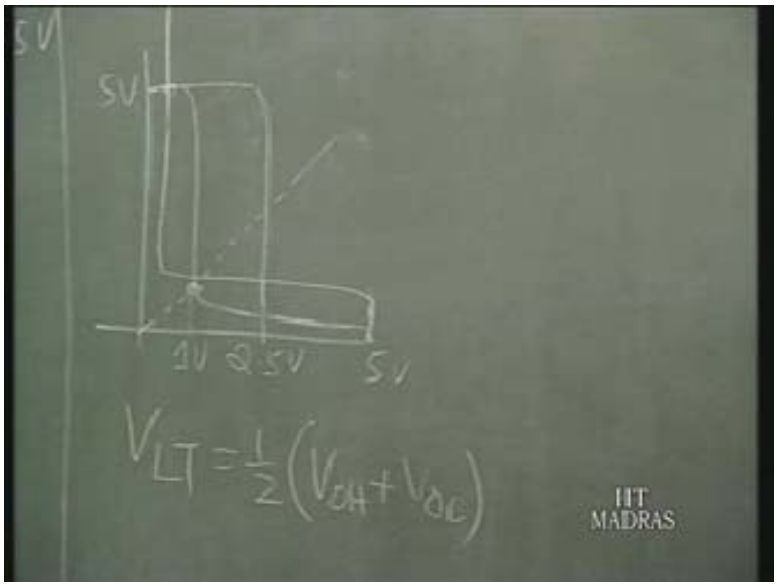

So it is always preferred, the ideal inverter characteristic would have the logic threshold some where midway between logic high and logic low. There you have in this case the noise margin high is this much, noise margin low is this much. So they are almost same so the ideal characteristics would have the logic threshold somewhere. So the logic threshold at half you can say ideally logic threshold should be half $V_{OH} + V_{OL}$ that would give you more or less symmetric margin. That is the logic swing what ever the logic swing is there it's properly utilized to have almost equal noise margin low and noise margin high. So this is also very important from the point of view of characteristics.

Finally the last point, the last characteristic which we have already pointed out is the fan out. The fan out is of a logic gate is the number of outputs you can connect from or the number of outputs or number of gates which it can drive basically. Suppose we have a NAND gate and we are connecting to large number of other gates. So this is the fan out, how many gates you are connecting to and this also there is a limit to it. So we shall take up that subsequently when we discuss the actual circuits. So there is a limit maximum limit for that. So that we hall next we shall take up actual circuits, start of with the actual logic circuits and discuss in terms of this characteristics which we have studied today.
Thank you.